Four steps to accelerate Monte Carlo applications

With background on the STAC-A2™ benchmark suite

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STAC-A2 in 5 minutes

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What is STAC-A2?

www.STACresearch.com/a2

- Benchmark suite
  - Specifications
  - Test-harness software
  - Vendor implementations – source & binary (“STAC Packs”)
- This version: Greeks on options
  - Options: Multi-asset, path-dependent, early exercise
  - Pricing model: Heston
  - Non-trivial Monte Carlo case
- Workloads
  - End-to-end calc of all Greeks
  - Each Greek in isolation
  - Component operations (e.g., square root, log, randoms)
- Measures:
  - Time per workload (speed)
  - Workload per time (capacity)
    - Scale dimensions: assets, paths, timesteps
  - Quality (agreement with theory)
  - Coming soon: workload per unit energy and space

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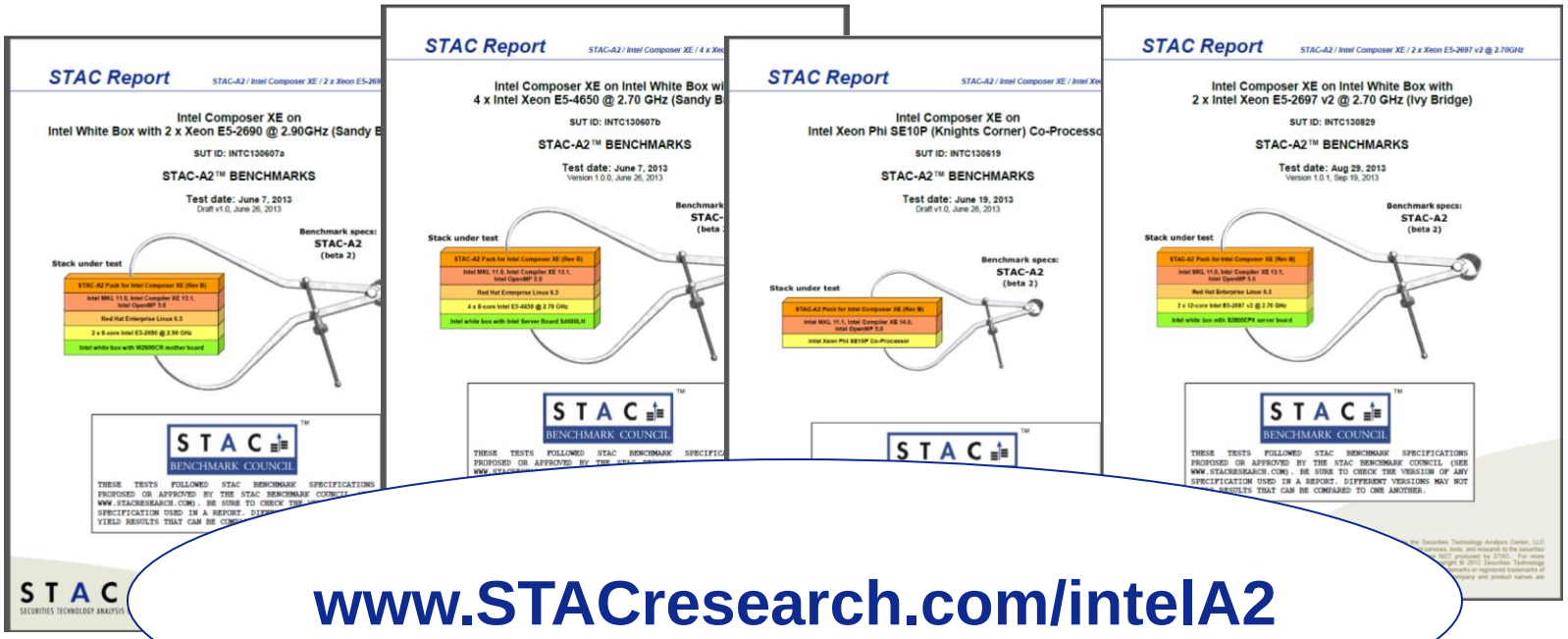
STAC-A2 status

- Version 1 nearing finalization
  - Results you'll see today are Beta2
  - Final specs expected in weeks
- Specs have been driven by major banks
- They are architecture neutral
- Major vendors are actively engaged
  - Intel, Nvidia, Altera, Calxeda

STAC-A2 pioneer vendor: Intel

- Four systems audited so far (Xeon and Phi)
  - Results are public
  - Config disclosures are in the STAC Vault (per policy)
  - STAC-A2 Pack for Intel Composer XE is in the STAC Vault (per policy)



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Four steps to accelerate Monte Carlo simulations in Finance

Andrey Nikolaev, SW Architect

Zhang Zhang, Technical Consulting Engineer

Intel

Four steps:

1. Consider upgrading your hardware
2. Apply Intel parallel programming model
3. Make sure your compiler/libraries/OS are optimized for the platform
4. Use tools to clarify bottlenecks

Performance Comparison of Intel Architectures
Scaling from generation to generation of IA platforms

Same code gives optimized performance on "IvyBridge" processor

STAC-A2 GREEKS Elapsed Time with Varying Number of Paths (Time in Seconds, Lower is Better)				
5 assets, 252 time steps	10,000 paths	25,000 Paths*	50,000 paths	100,000 paths
Intel® Xeon® E5-2690 16 cores	2.87	7.11	14.12	28.52
Intel® Xeon® E5-4650 32 cores	2.10	5.30	10.17	24.27
Intel® Xeon Phi™ B0-ES2, 61 cores	3.87	6.49	13.32	26.67
Intel® Xeon® E5-2697 V2, 24 cores	1.95	4.82	9.44	19.73

Intel SW tools help to seamlessly scale STAC-A2 benchmark from gen-to-gen of IA

CPU System configurations:

- Intel® Xeon® Processor E5-4650, 4 Eight-Core CPUs (20MB LLC, 2.7GHz), 64GB of RAM, HT off, EIST on, TURBO on.
- Intel® Xeon® Processor E5-2690, 2 Eight-Core CPUs (20MB LLC, 2.9GHz), 64GB of RAM, HT off, EIST on, TURBO on.
- Intel® Xeon® Processor E5-2697, 2 Twelve-Core CPUs (30MB LLC, 2.9GHz), 64GB of RAM, HT off, EIST on, TURBO on.
- Operating system: RHEL* 6 GA x86_64 (Linux* kernel 2.6.32)
- Intel® Composer XE 2013.3.163
- Benchmark source: STAC®

Co-processor system configuration:

- Intel® Xeon Phi™ Coprocessor ES2, step B0, 61 cores (30.5MB total cache, 1.1 GHz),
- 8GB GDDR5 memory. Intel® Manycore Platform Software Stack (MPSS) 2.1.4346.
- Intel® Composer XE 2013.sp1_beta.0.0151
- Benchmark source: STAC®

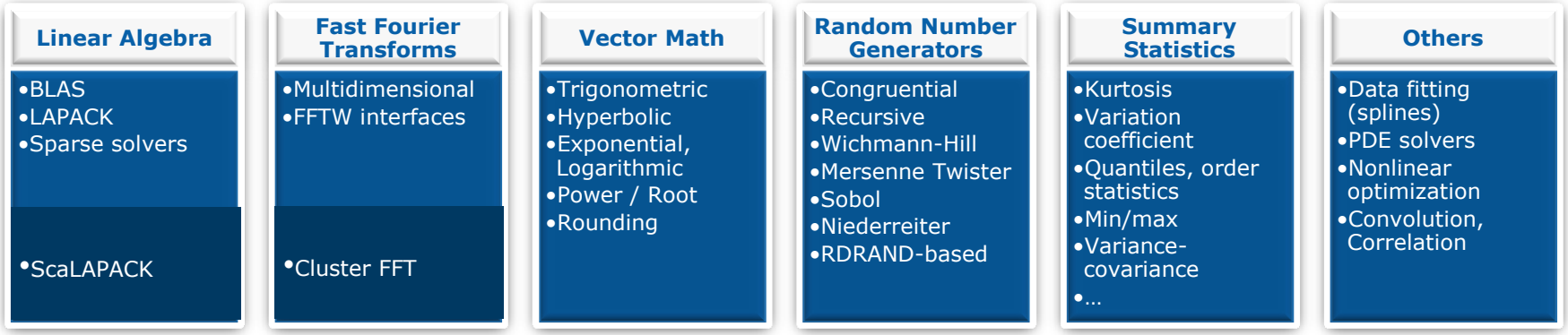
* Baseline problem size. These values correspond to GREEKS.TIME benchmarks and represent the average of 5 runs (1 cold run followed by 4 warm runs). Other results in this table are single (cold) runs only.

Apply the Intel parallel programming model

Cores	• Parallelization with OpenMP*
Vectors	• Compiler based vectorization
Data blocking	• Use caches to hide memory latency • Organize memory access for data reuse
Data layout and alignment	• Structure of arrays facilitates vector loads / stores, unit stride • Align data for better vectorization

Use A Highly Optimized Math Library

Intel® MKL - Industry's leading math library [1]



Intel® MKL functions used in the STAC-A2 implementation:

- RNG: MCG59, Gaussian distribution with ICDF
- Matrix operations: TRMM, Cholesky
- Summary statistics: Mean, Correlation
- Splines: Data fitting
- Vector math functions

[1] *2011, 2012, 2013 Evans Data N. American developer survey*

Use An Optimizing Compiler

Vectorization: `#pragma ivdep`

- Vectorization diagnostic: `-vec-report=5`
- Even some loops with irregular accesses are vectorized.

Parallelization (threading): Intel® OpenMP

Optimized scalar math functions:

- `sqrt, log, exp, div, erf`

Accuracy optimization: `-fimf-precision=low:sqrt`

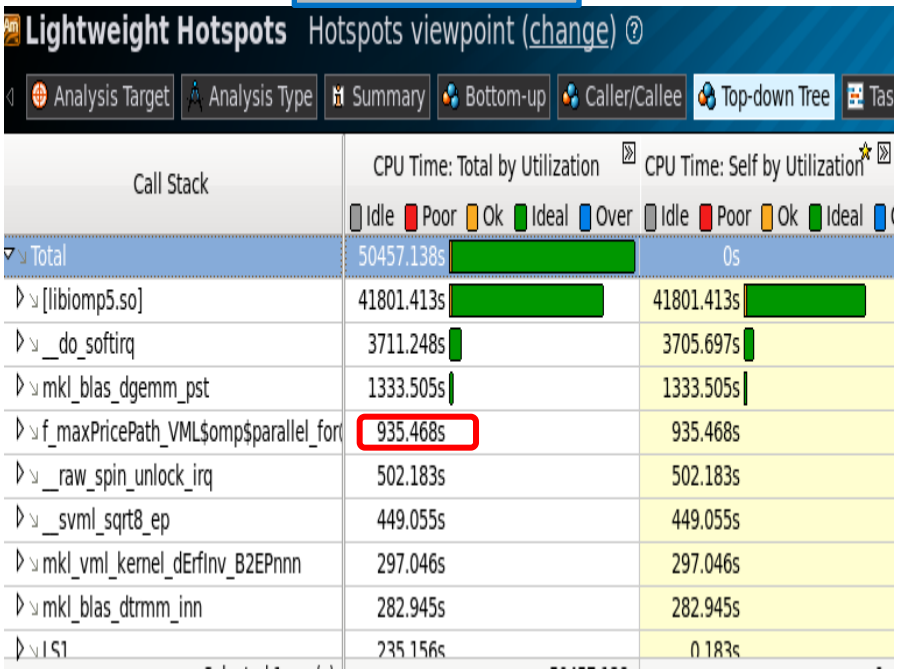
- Trade accuracy for performance (sqrt only).

Domain exclusion: `-fimf-domain-exclusion=31`

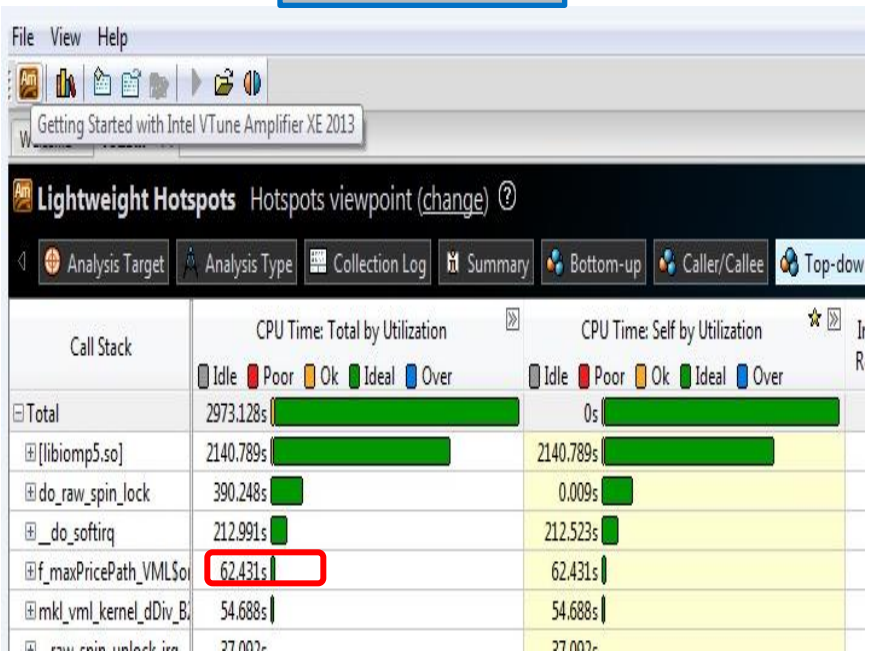
- No handling for nans, infinities, extremes, denormals, etc.

Finding Performance Bottlenecks
Intel® VTune™ Amplifier XE

2012 version



2013 version



Intel® VTune™ Amplifier helped to identify and fix hotspots

- Tuned PATHGEN ~ 15x faster than in 2012 version
- Additionally tuned Intel MKL trmm function – not the hotspot

Result: "Old" Code vs. "New" Code

After recompilation the same code runs faster on Intel® Xeon® CPUs

	STAC-A2.β2.GREEKS Elapsed Time, seconds (25,000 Paths, 5 Assets, 252 Time steps)			STAC-A2.β2.GREEKS Elapsed Time, seconds (50,000 Paths, 10 Assets, 126 Time steps)		
	Intel® Xeon® E5-2690 16 cores	Intel® Xeon® E5-4650 32 cores	Intel® Xeon Phi™ B0-ES2, 61 cores[1]	Intel® Xeon® E5-2690 16 cores	Intel® Xeon® E5-4650 32 cores	Intel® Xeon Phi™ B0-ES2, 61 cores[1]
2012 version	11.43	8.93	98.43	65.28	43.43	na[2]
2013 version	7.14	5.16	6.49	37.50	22.40	27.22
Performance gain	1.60x	1.73x	15.17x	1.74x	1.94x	

System configurations:

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- 8GB GDDR5 memory. Intel® Manycore Platform Software Stack (MPSS) 2.1.4346.
- Intel® Composer XE 2013.sp1_beta.0.0151
- Benchmark source: STAC®

[1] 2012 version with improved work w/ memory

[2] application terminated due to memory limitation

How did we improve code for nearly 2x speedup on Xeon?

Critical Performance Tunings

Memory optimization

- In-place computation minimizes footprint and data copying.

Cache optimization

- Blocking for L1 cache

Thread affinity to prevent thread migration

- `KMP_AFFINITY=compact`

Optimization for Path Generation
Parallelization and Vectorization

```
… = (double*)_mm_malloc(size, 64);
… = (double*)_mm_malloc(size, 64);


  // Preprocessing: computing parameters …
  …

  #pragma omp parallel for default(shared)
  for(J=0;J<path_blocks;J++)
  {
     …

     for(i=0;i<timeSteps-1;i++)
     {
        …

        #pragma ivdep
        #pragma noprefetch
        for(j=0;j<jn_j0;j++)
        {
             …
             …
        }
     }
  }
  …
```

Align arrays on 64-byte boundaries

Parallelize the outer loop using OpenMP

Vectorize the inner loop with Intel compiler pragmas

Optimization for Path Generation
Using Intel® MKL Random Number Generator

```
…
#pragma omp parallel for default(shared)
for(J=0;J<path_blocks;J++)
{
   …
   vslNewStream(&stream, VSL_BRNG_MCG59, seed);
   vslSkipAheadStream(stream,
                      J*block_size*processes*(timeSteps-1));

   for(i=0;i<timeSteps-1;i++)
   {
      …
      vdRngGaussian(GAUSSIAN_METHOD, stream,
                    processes*jn_j0, mRng, 0.0, 1.0);
      …
      #pragma ivdep
      #pragma noprefetch
      for(j=0;j<jn_j0;j++)
      {
          …
          …
      }
    }
}
…
```

Initialize an RNG stream. Block-split among threads.

Generate all random numbers to be used in each time step.

Optimization for Path Generation
The Inner loop

```
…
#pragma omp parallel for default(shared)
for(J=0;J<path_blocks;J++)
{
   …

   for(i=0;i<timeSteps-1;i++)
   {
      …
      #pragma ivdep
      #pragma noprefetch
      for(j=0;j<jn_j0;j++)
      {
          Z1 = mRng1[j]; Z2 = mRng2[j];
          V0 = mV[k*jn_j0_2 + j + j_block_shift];
          W  = (Z2 - Z1 * rho) * _inv_1_m_rho_sq;
          …
          b2  = m * m * (2.0 + sqrt( 4.0 - 2.0 * psi )) / s2 - 1.0;
          b   = sqrt(b2);
             if( logPricePathPtr[ j_block_shift + j ] < Y1 )
             {
                      logPricePathPtr[ j_block_shift + j ] = Y1;
             }
          mY[k*jn_j0_2 + j_block_shift + j] = Y1;
          mV[k*jn_j0_2 + j_block_shift + j] = V1;
          …
      }
```

Use vectorized version of sqrt from compiler library with domain-exclusion

Start Today

- Review the audited reports at www.STACresearch.com/intelA2
- Get the STAC-A2 Pack for Intel Composer XE and the STAC-A2 Tools & Specs at www.STACresearch.com/a2
- Run STAC-A2 on your systems

Links:

- Access the Intel Tools with Intel C++ compiler/MKL/VTune Amplifier:

  http://www.intel.com/content/www/us/en/servers/server-products.html

  http://www.intel.com/content/www/us/en/software-developers/software-developers.html

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Q&A

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2. Andersen, L. 2007. Efficient Simulation of the Heston Stochastic Volatility Model. Available at SSRN : //ssrn.com/abstract=946405

3. www.STACresearch.com/intelA2

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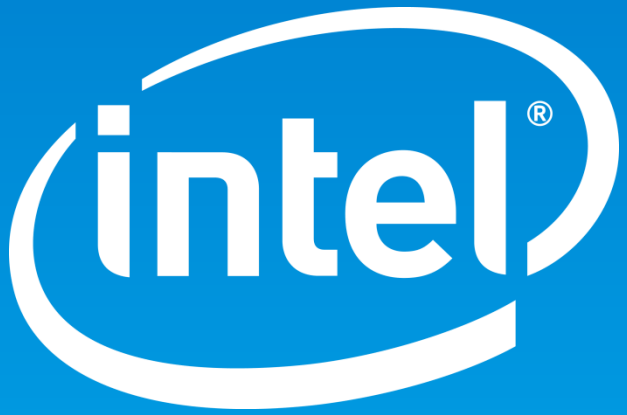
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