



METAMAKO

Metamako Platforms

Robust, Flexible, Controllable

Dr David Snowdon
CTO

Simplifying networks
Reducing latency in Electronic Trading
Opening up network packet visibility
Increasing flexibility

Updates

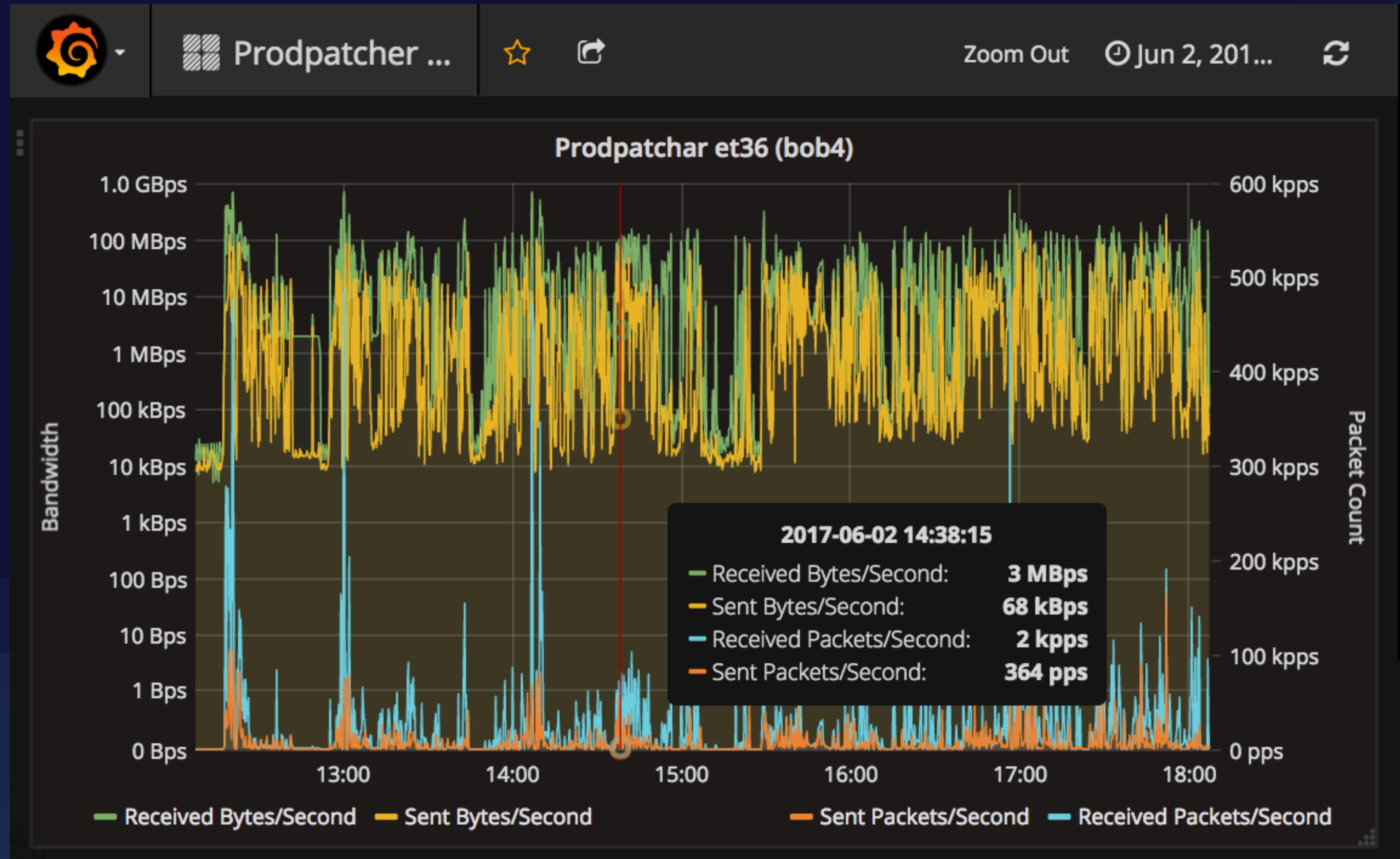
Some **big updates**

- Major MetaWatch improvements
- 1G
- Filtering
- Rubidium clock
- Time-series data
- JSON-RPC API
- Experimental BGP/PIM

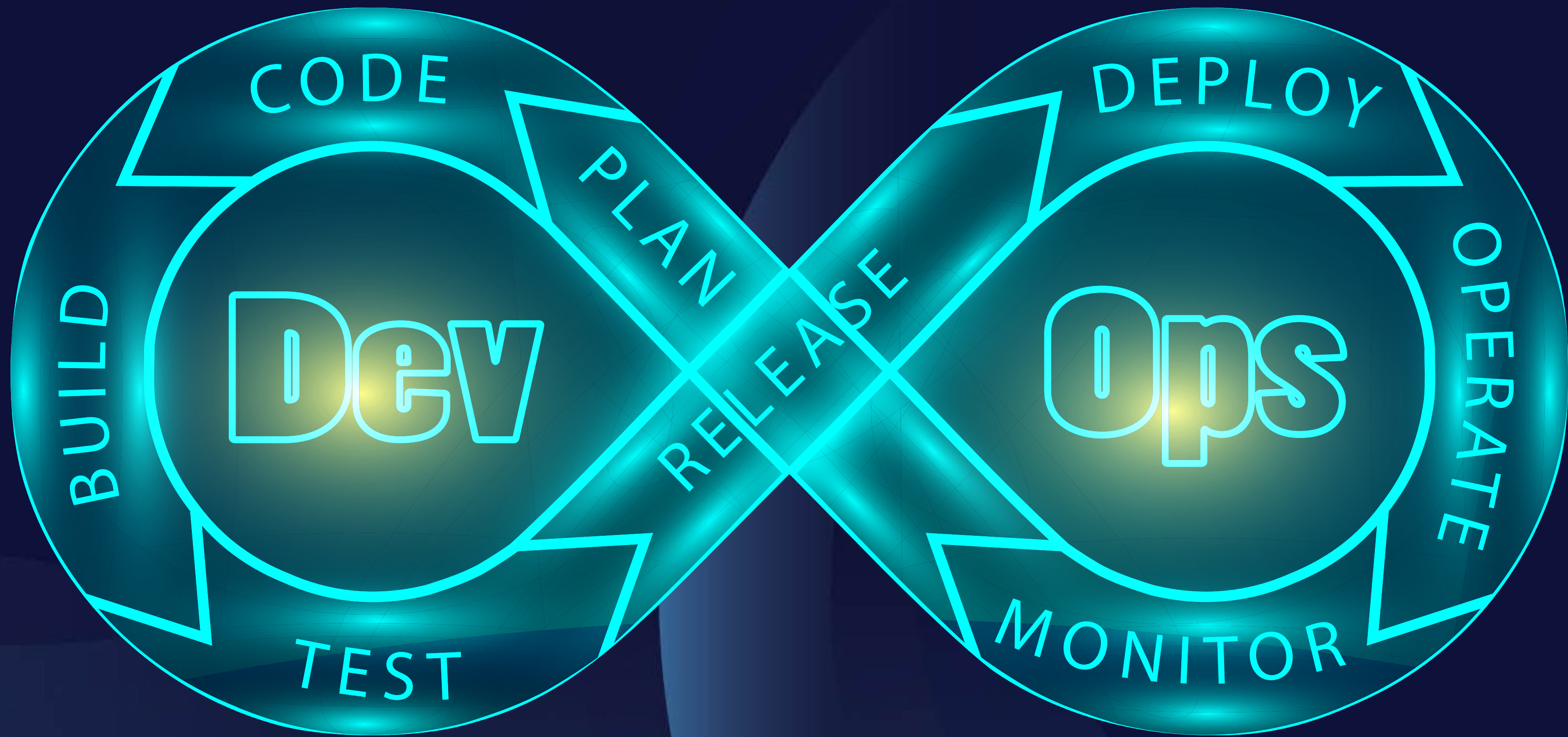
mos-0.14.0beta1 released today.



Some big updates



Some big updates



Devops with a JSON-RPC API

MetaConnect 96



MetaConnect 96



- 96 front panel ports
- Between 5 and 6 ns latency (Not STAC Benchmark)
- FPGA-enabled variants, Optional OCXO/Rb/GPS upgrade.
- Runs apps: MetaWatch, MetaMux, MetaFilter... more to come.

FPGA Platforms

FPGA Development Platforms



MetaApp 32



MetaMux 48



MetaConnect 96

FPGA Development Platforms

K-Series Devices Virtex 7



MetaApp 32



MetaMux 48K



MetaConnect 96K

C-Series Devices Arria 10



MetaApp 32C



MetaMux 48



MetaConnect 96C

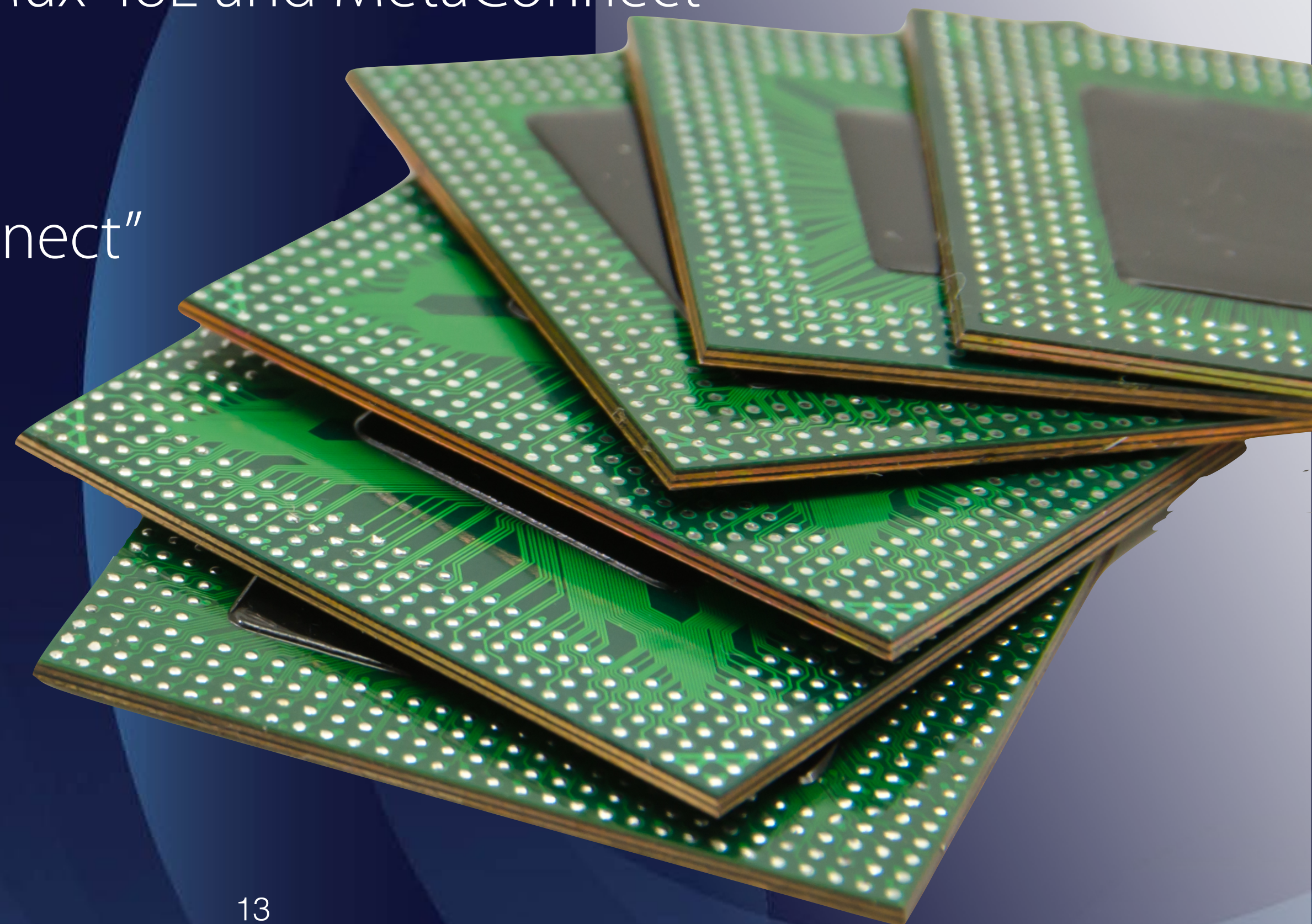
FPGA Development Platforms

- Development kit, example designs, tips and tricks:

www.metamako.com/support

Announcing E-Series

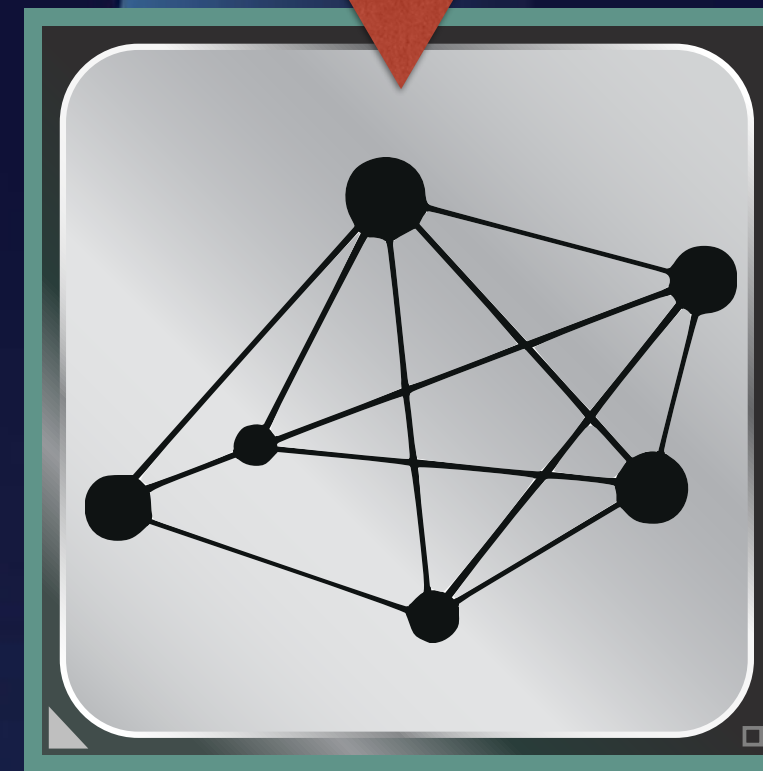
- **Ultrascale** and **Ultrascale+** FPGA
- MetaApp 32E, MetaMux 48E and MetaConnect 96E
- All include “MetaConnect”



FPGA

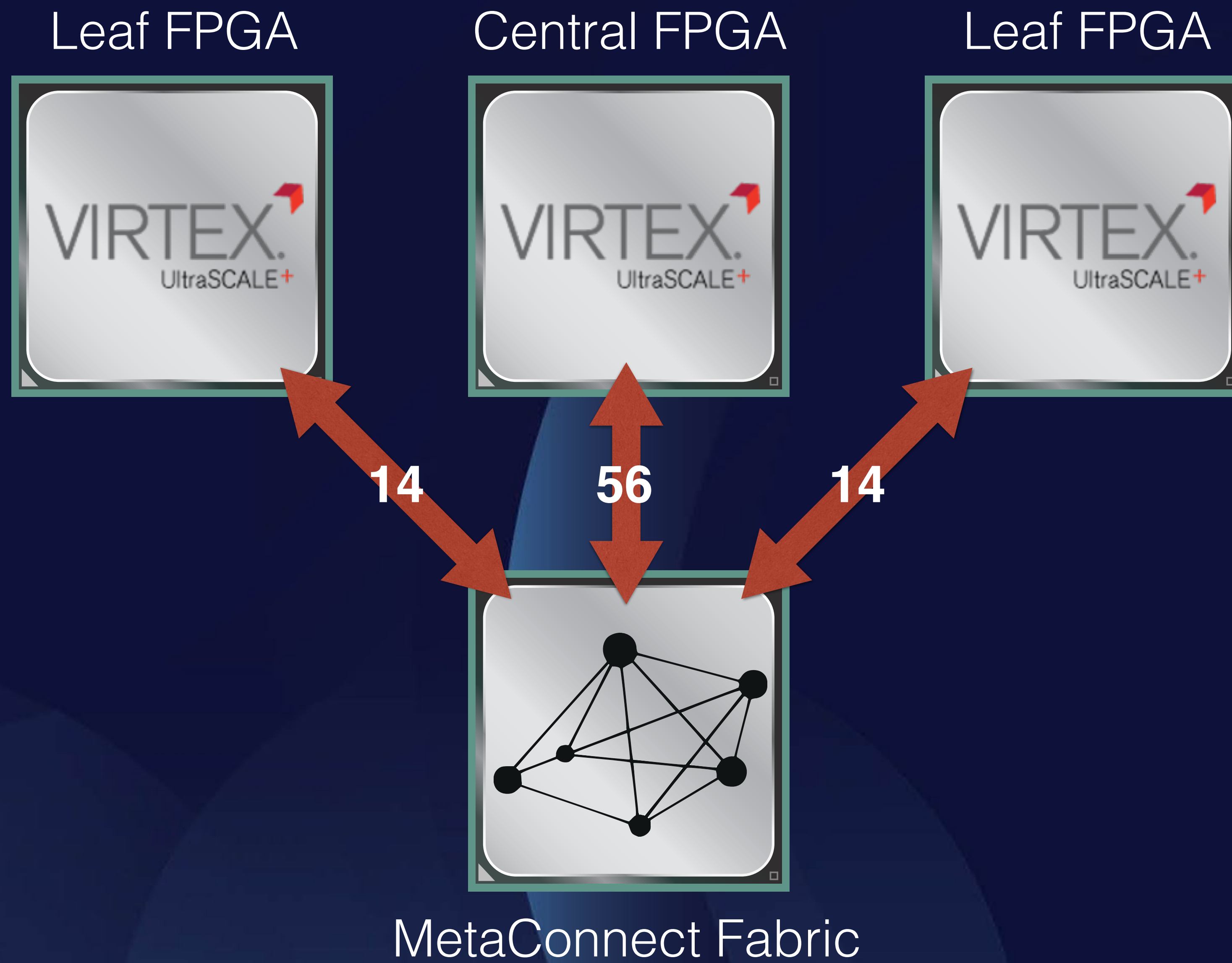


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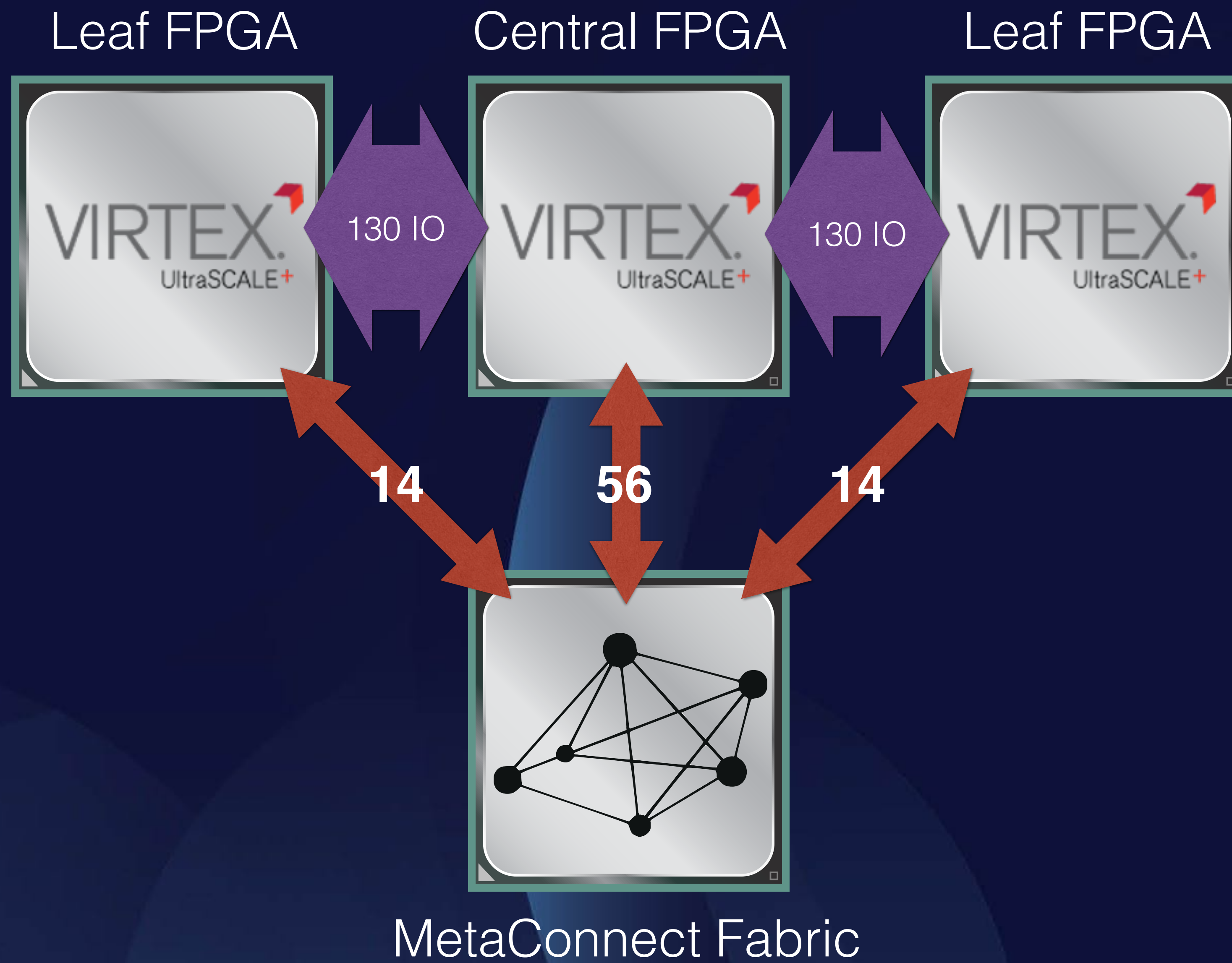


MetaConnect Fabric

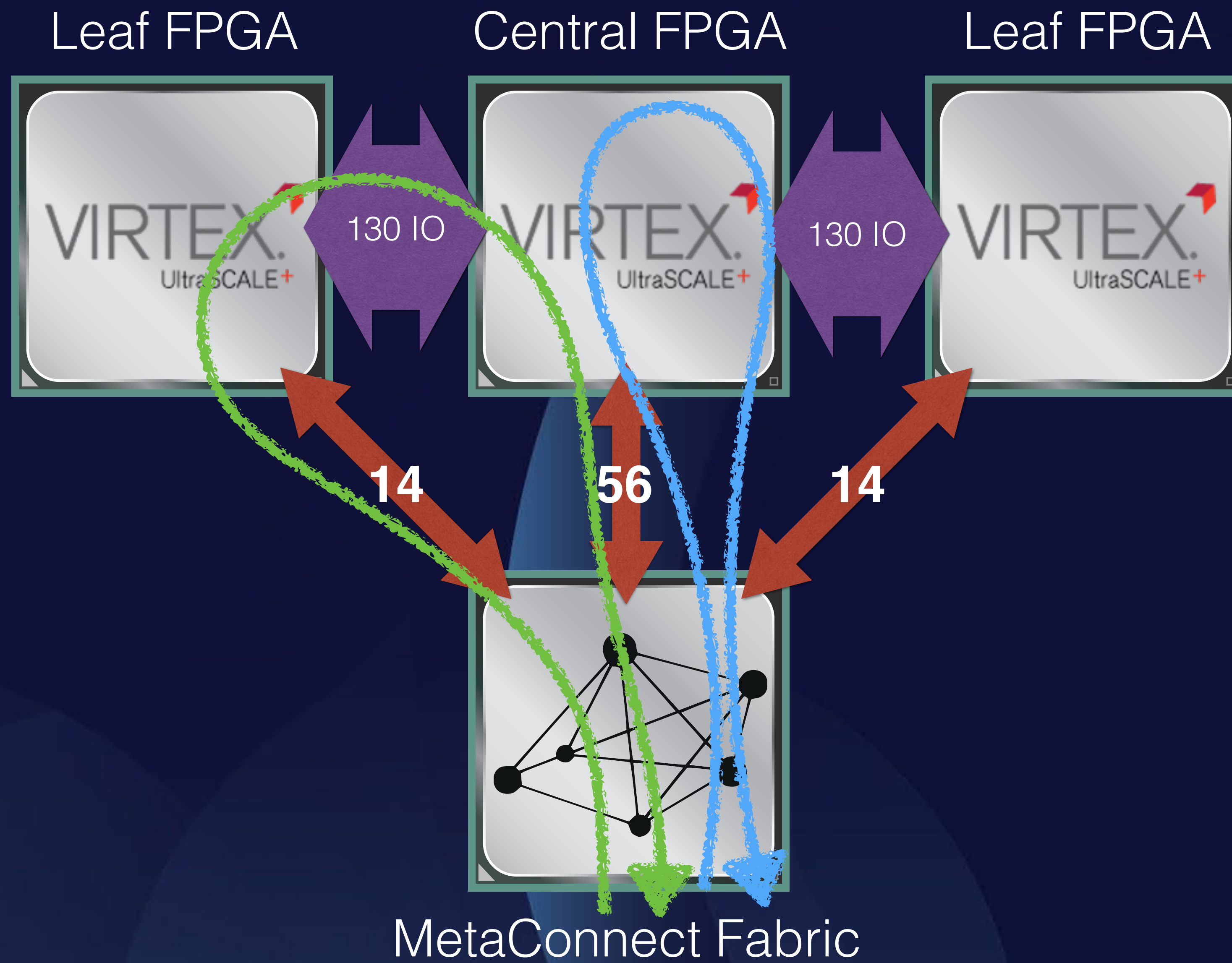
E-Series

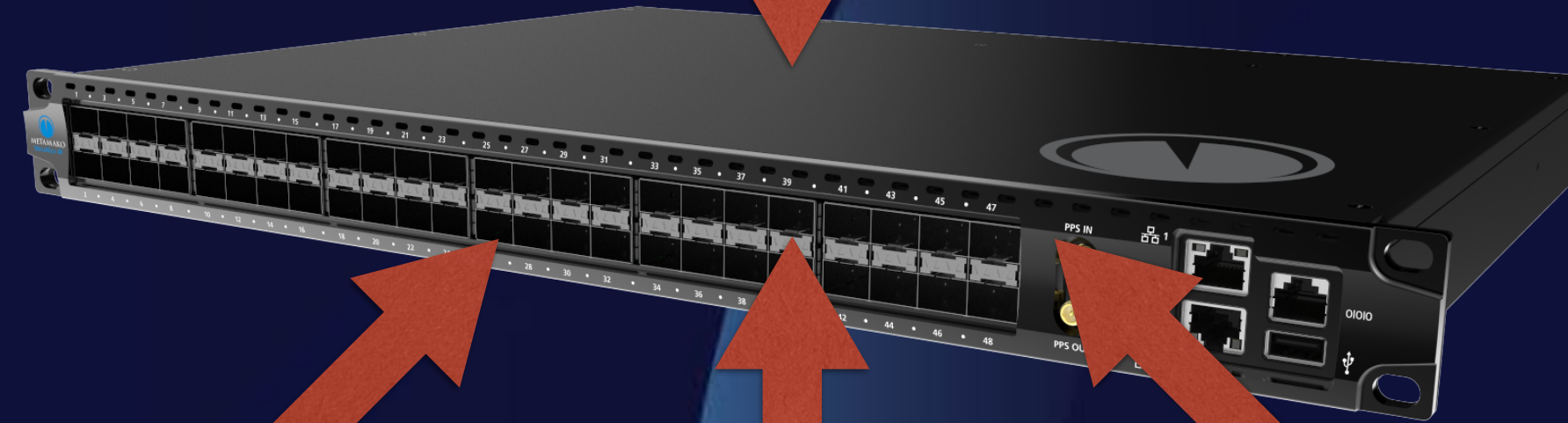


E-Series



E-Series





MetaMux 48E



	K-Series (Virtex 7 415T)	C-Series (Arria 10)	E-Series (3x VU9P Variant)
Flip Flops or Registers	515k	1,708k	7,092k
Total On-Chip RAM	31.7 Mb	65Mb	1,037 Mb



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For development kits, see:
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