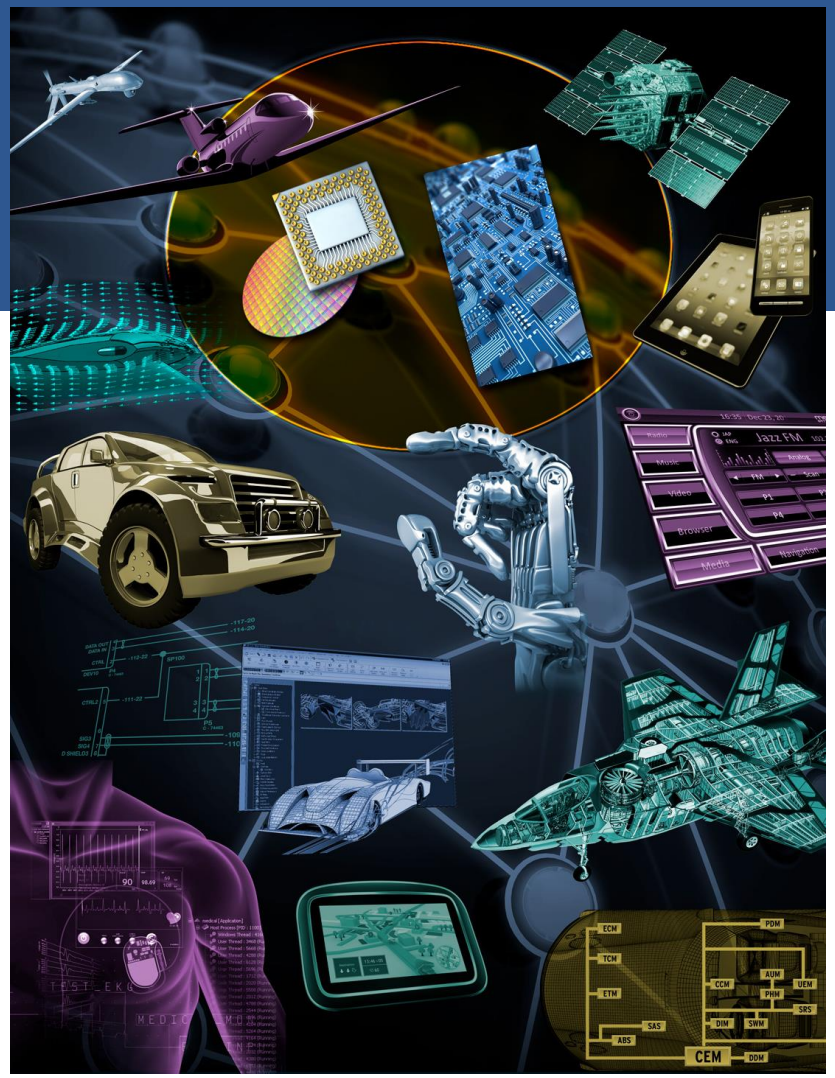

Demystifying FPGA Design and Verification

Harry D. Foster

Chief Scientist Verification

Design Verification Technology

June 5, 2017

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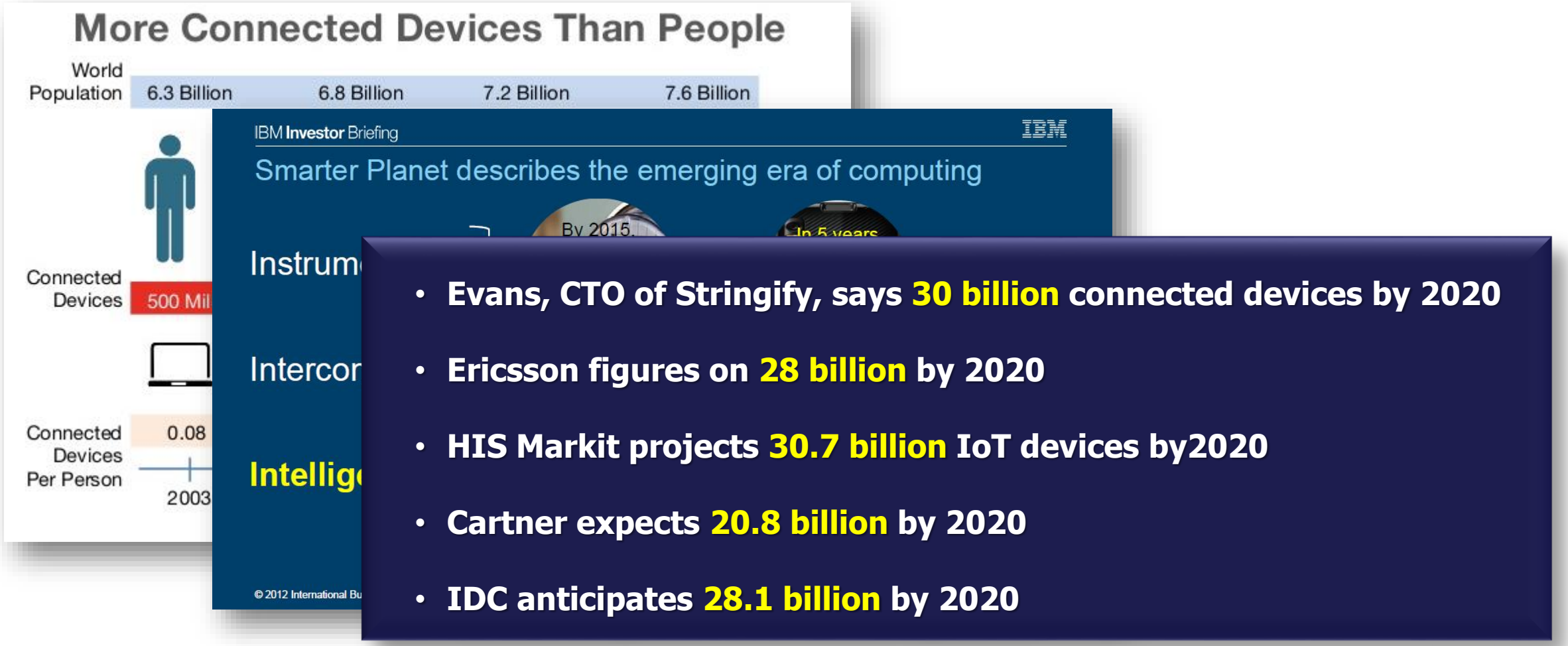
THE ERA OF DIGITAL INTELLIGENCE

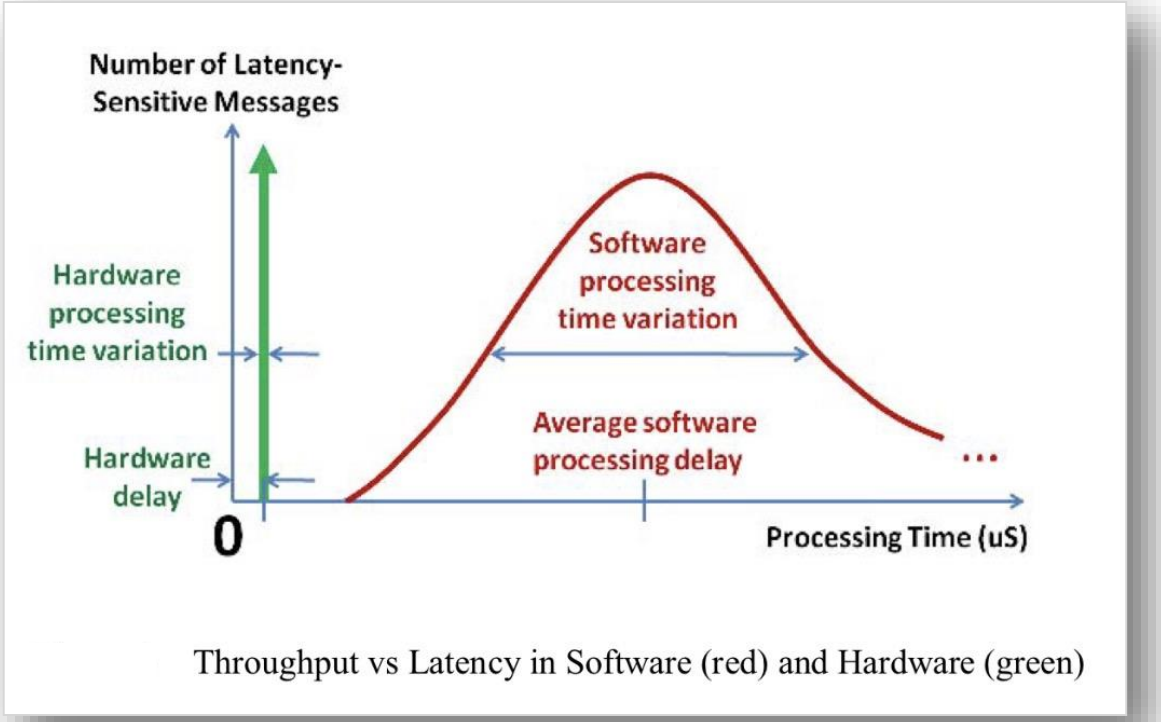
Everything Connected and in the Cloud



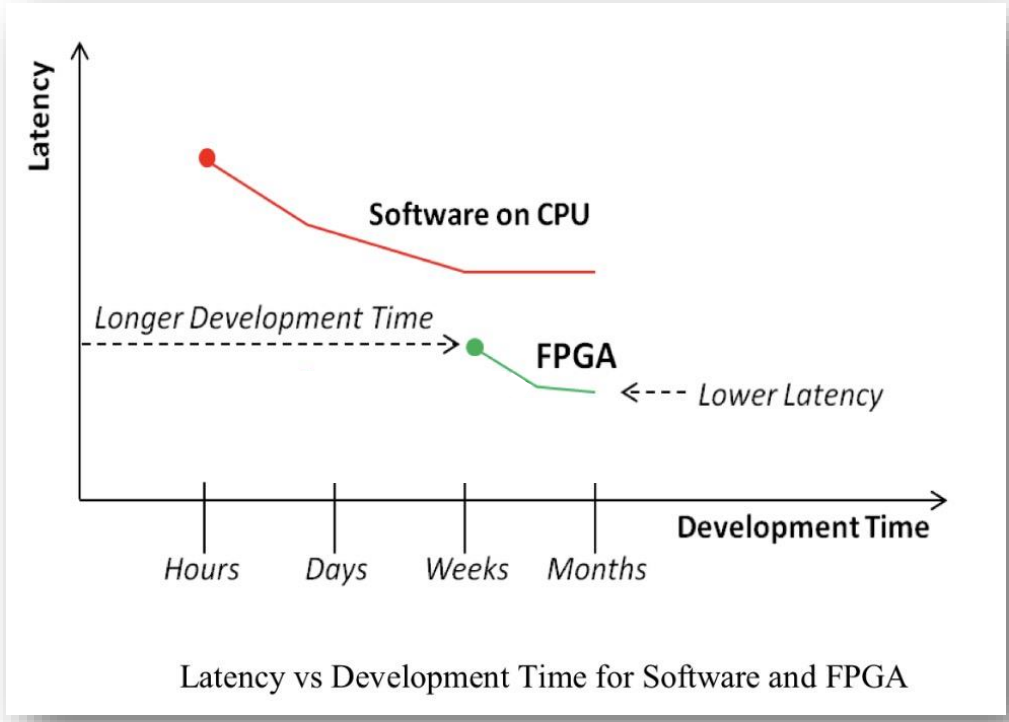

Low Latency
FPGA-Based Acceleration
Real-Time Compute
REALLY BIG DATA & FAST DATA
Security
Machine Learning
High Availability

Advantages of FPGA-Based Accelerator Platforms

Competitive Advantage Through Low Latency and Faster Compute



Throughput vs Latency in Software (red) and Hardware (green)

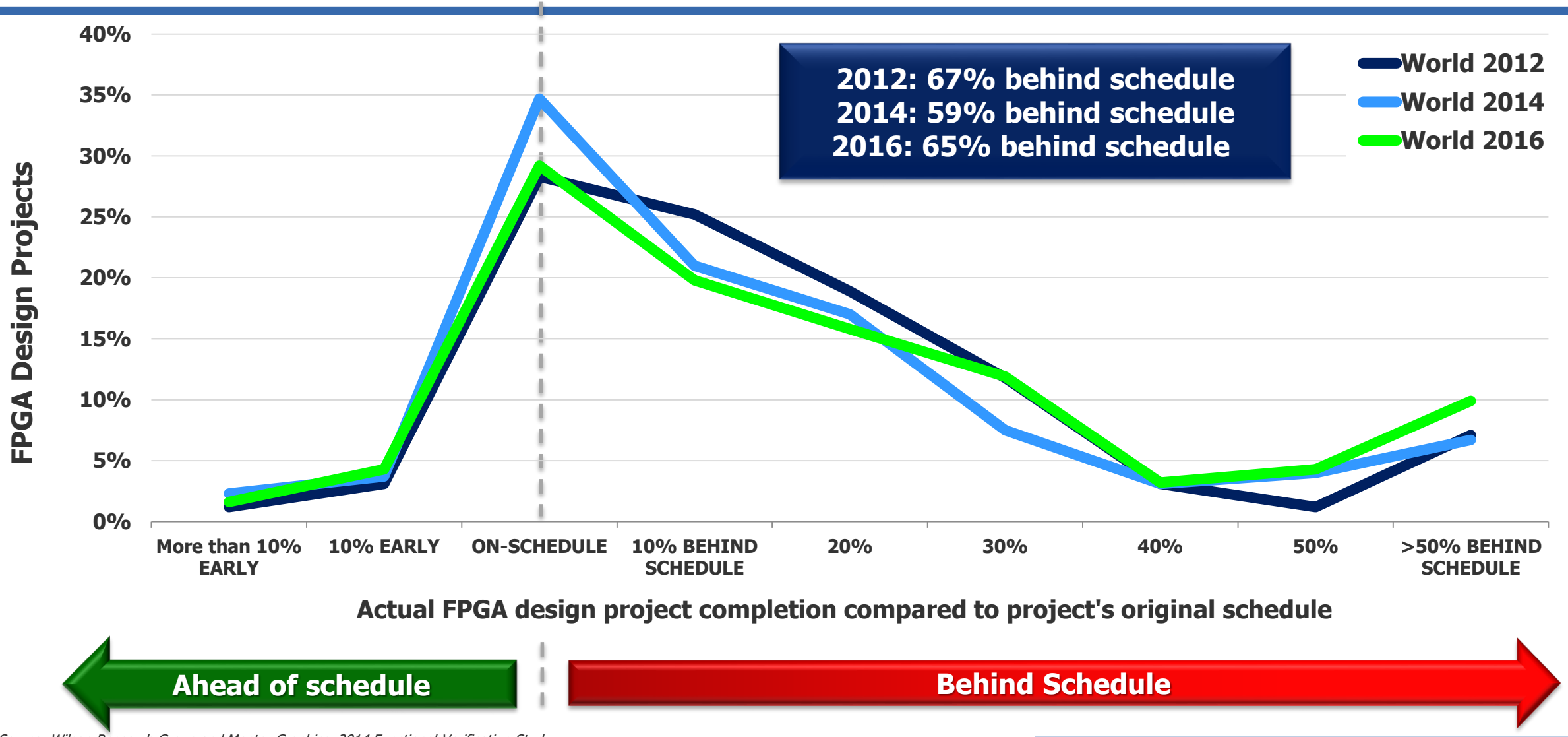


Latency vs Development Time for Software and FPGA

Source: A low-latency library in FPGA hardware for High-Frequency Trading (HFT), 2012 IEEE 20th Annual Symposium on High-Performance Interconnect

The Need to Shift Left

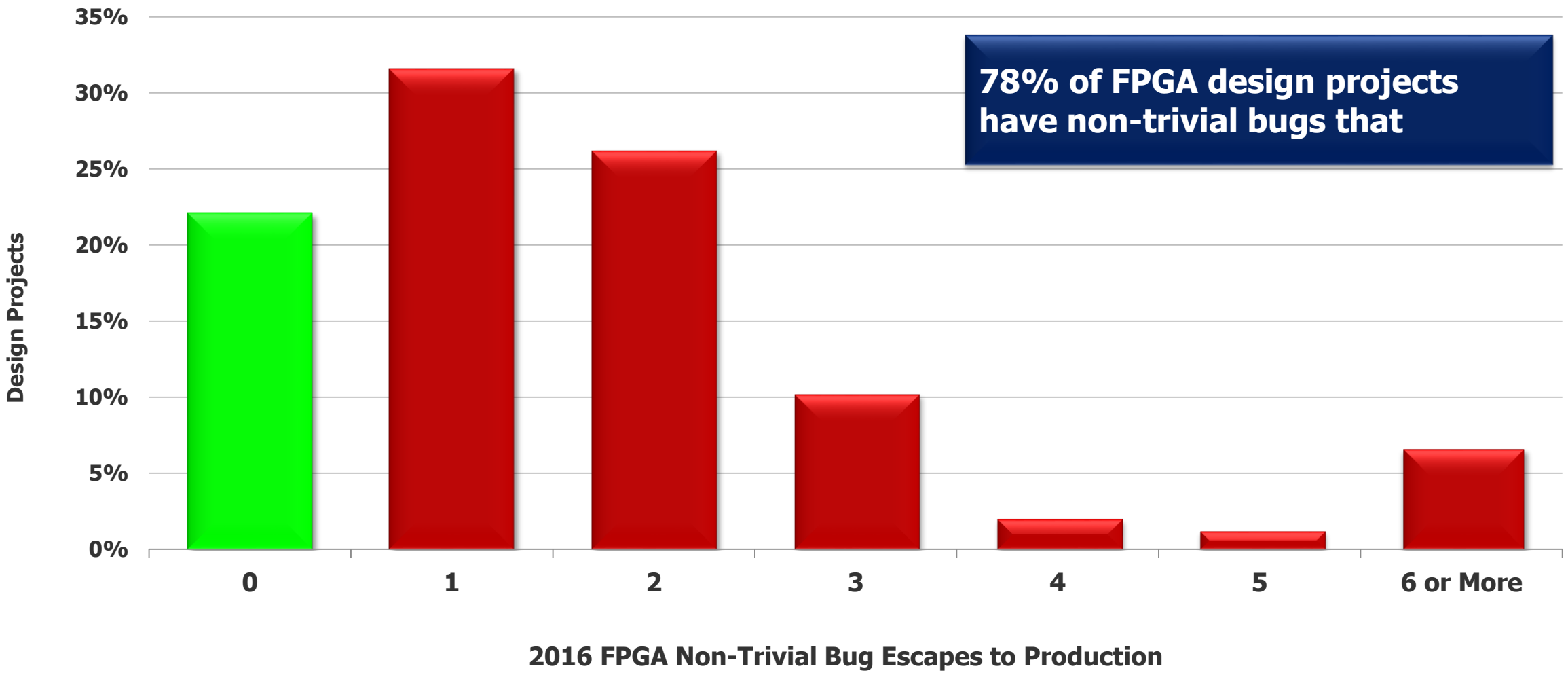
Characteristics of Projects Who Meet or Exceed Schedule



Source: Wilson Research Group and Mentor Graphics, 2014 Functional Verification Study

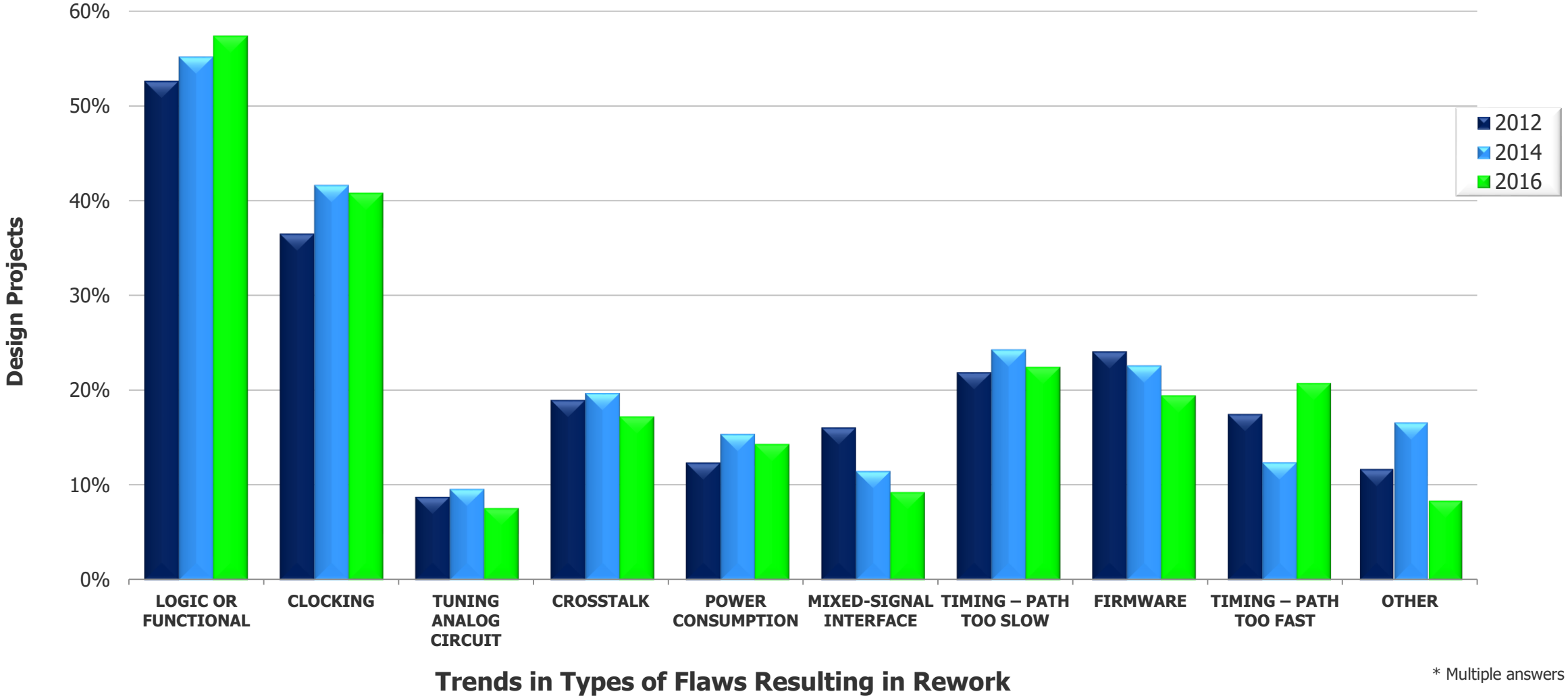
The Need to Be Green

Characteristics of Projects Without Bug Escapes



Source: Wilson Research Group and Mentor Graphics, 2016 Functional Verification Study

Flaws Contributing to FPGA Rework



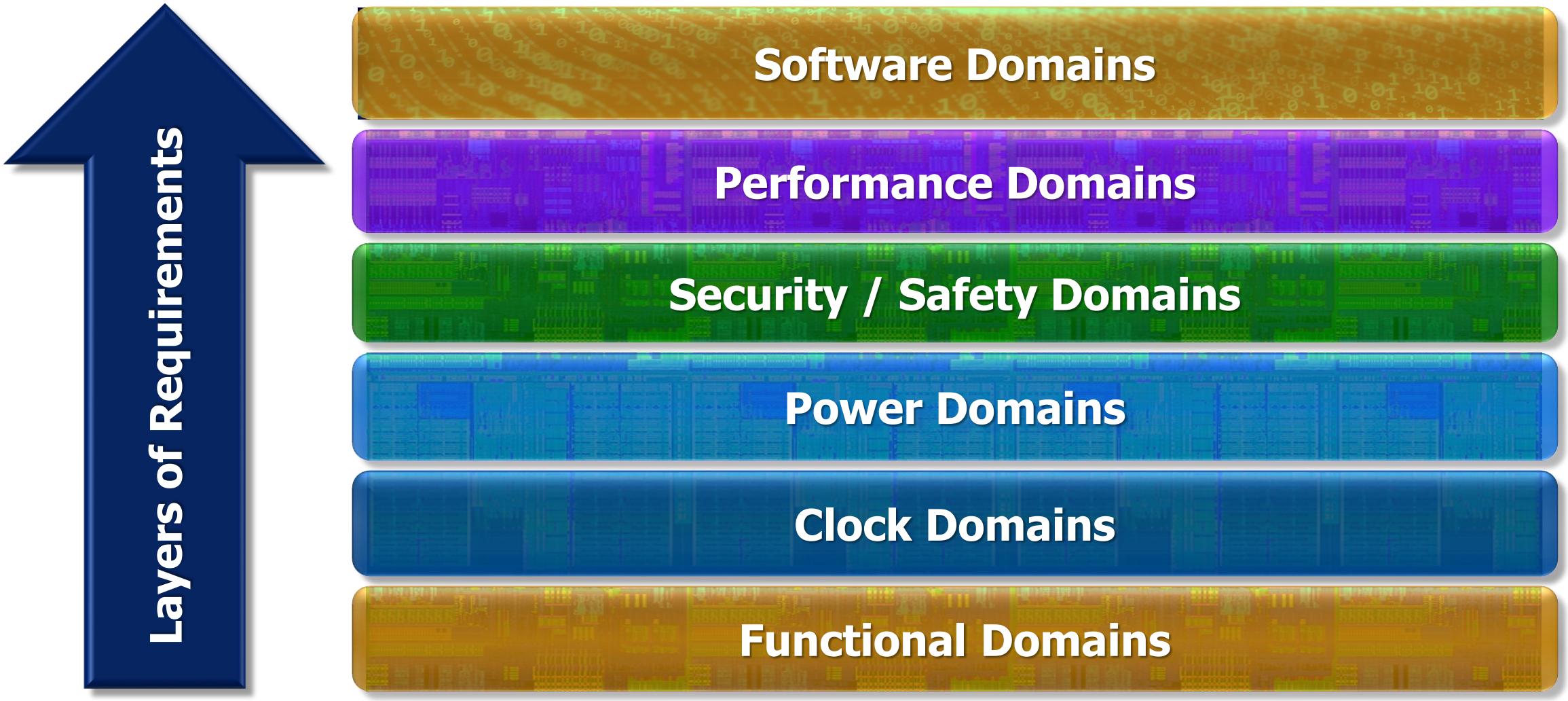
Trends in Types of Flaws Resulting in Rework

* Multiple answers possible

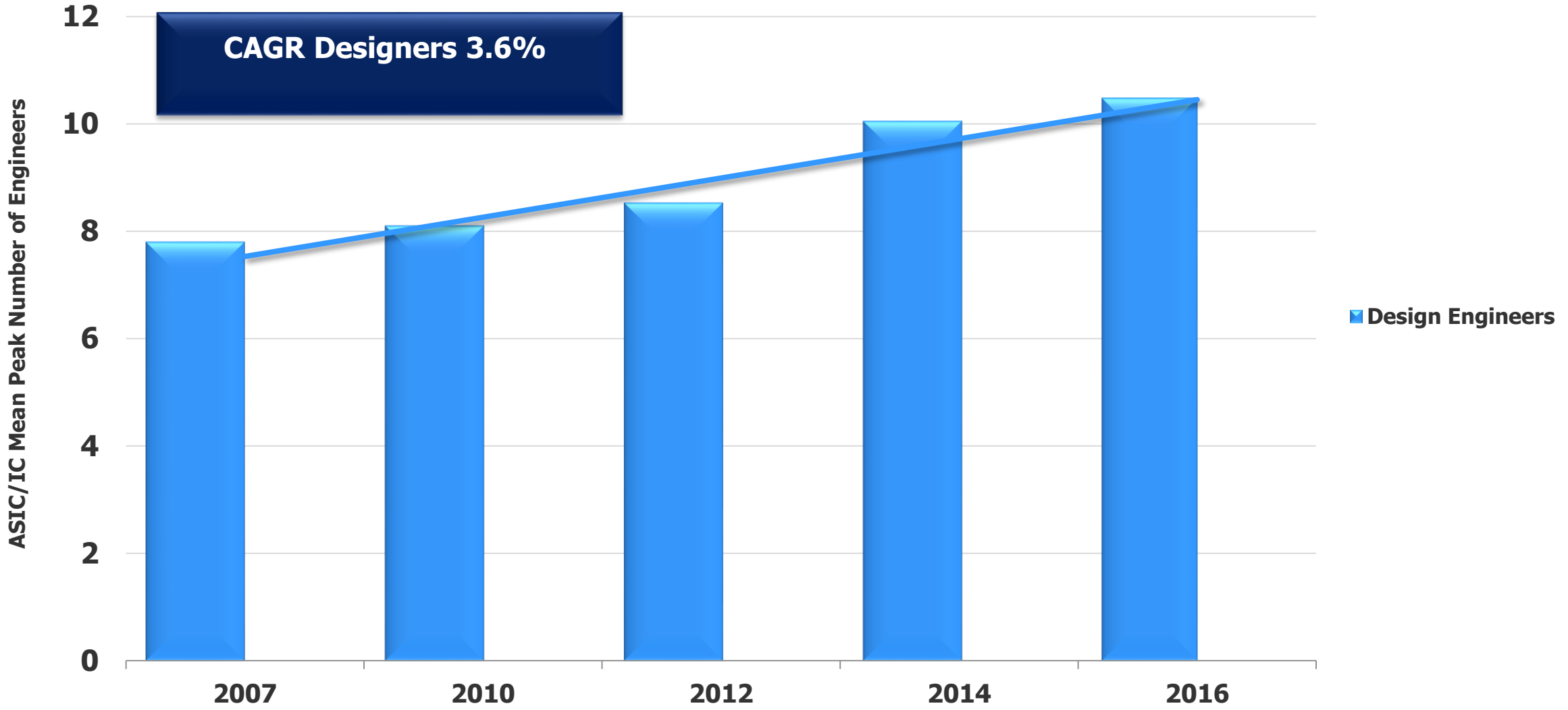
Source: Wilson Research Group and Mentor Graphics, 2016 Functional Verification Study

RISING VERIFICATION COMPLEXITY

The Emergence of New Layers of Verification Requirements Brought on by the System Era



Demand for Design Engineers Grows Slowly



Source: Wilson Research Group and Mentor Graphics, 2016 Functional Verification Study

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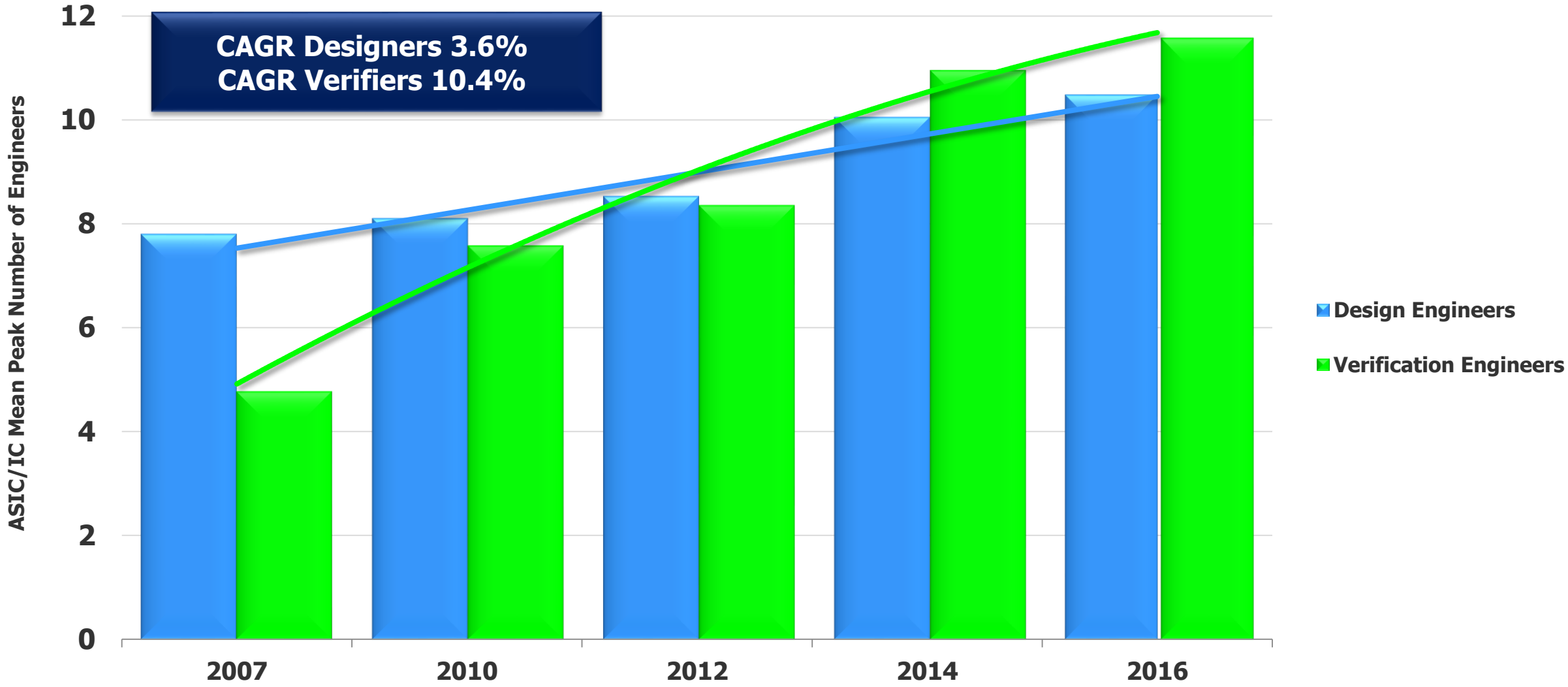
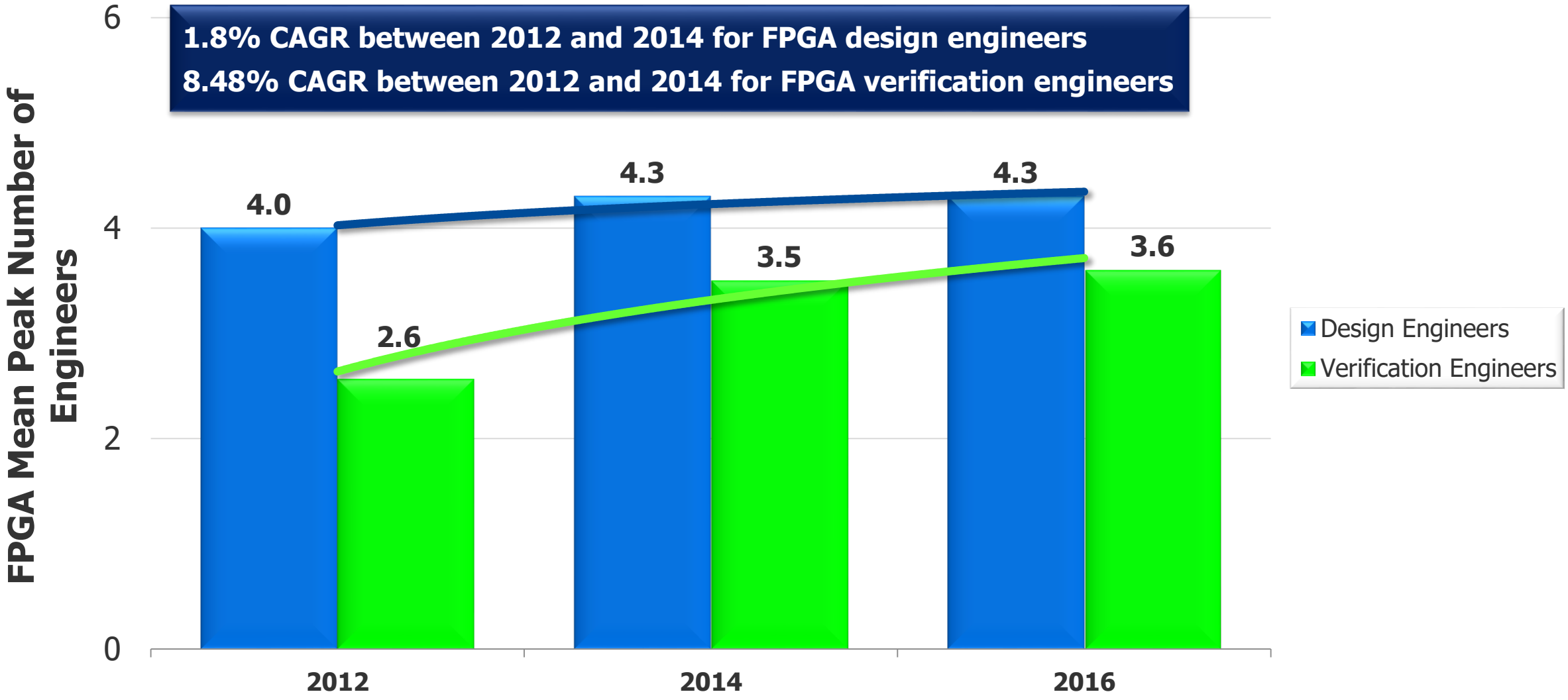
But what about Verification Productivity?



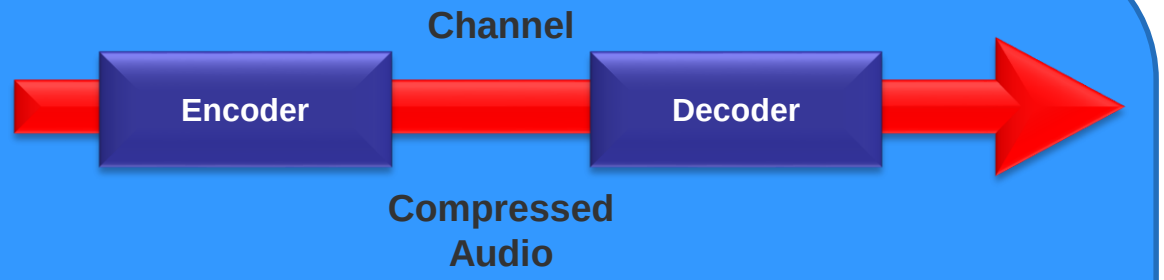
Source: Wilson Research Group and Mentor Graphics, 2016 Functional Verification Study

About a 1-to-1 Ratio of FPGA Verification and Design Engineers

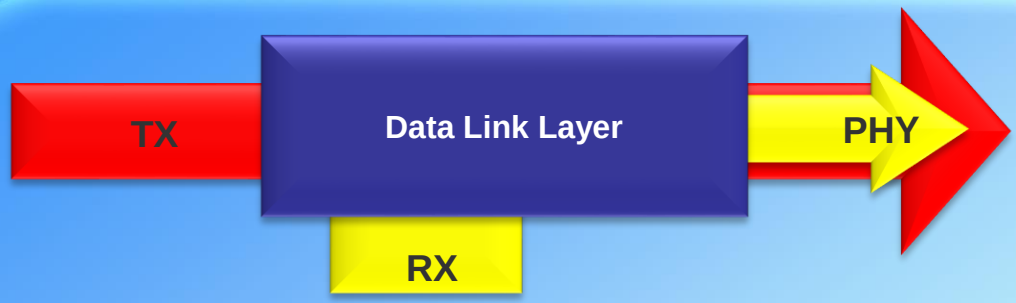


Source: Wilson Research Group and Mentor Graphics, 2016 Functional Verification Study

What Makes Functional Verification Difficult?



- Single, sequential data streams
  - Floating point unit
  - Graphics shading unit
  - DSP convolution unit
  - MPEG decode
  - . . .



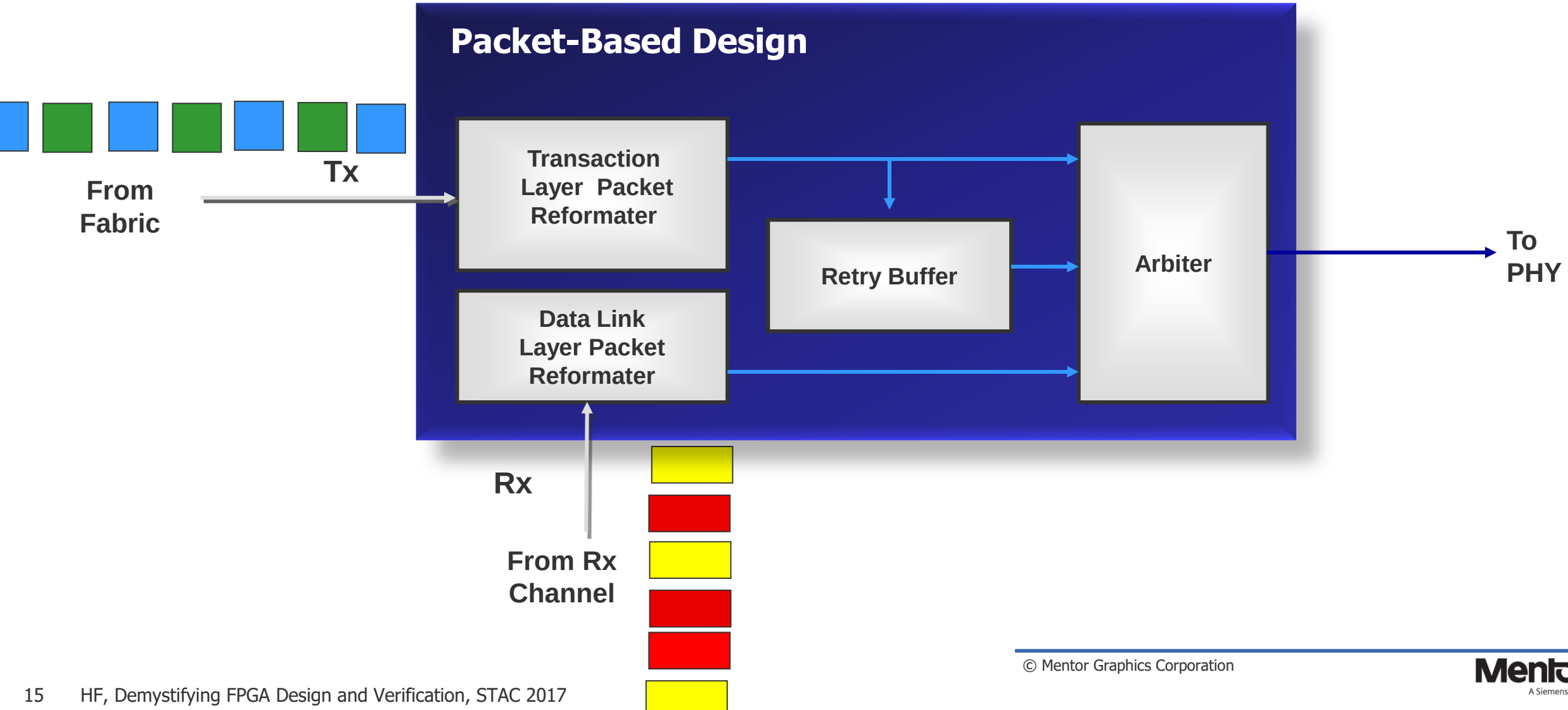
- Multiple, concurrent data streams
  - Cross bar
  - Bus traffic controller
  - DMA controller
  - Standard I/F (e.g., PCIe)
  - . . .

Sequential data streams
1x **number of bugs**

Concurrent data streams
5x **number of bugs**

-Ted Scardamalia, internal IBM study

Verifying Concurrency Requires Appropriate Solutions



Finding Corner Case Bugs Requires Appropriate Solutions

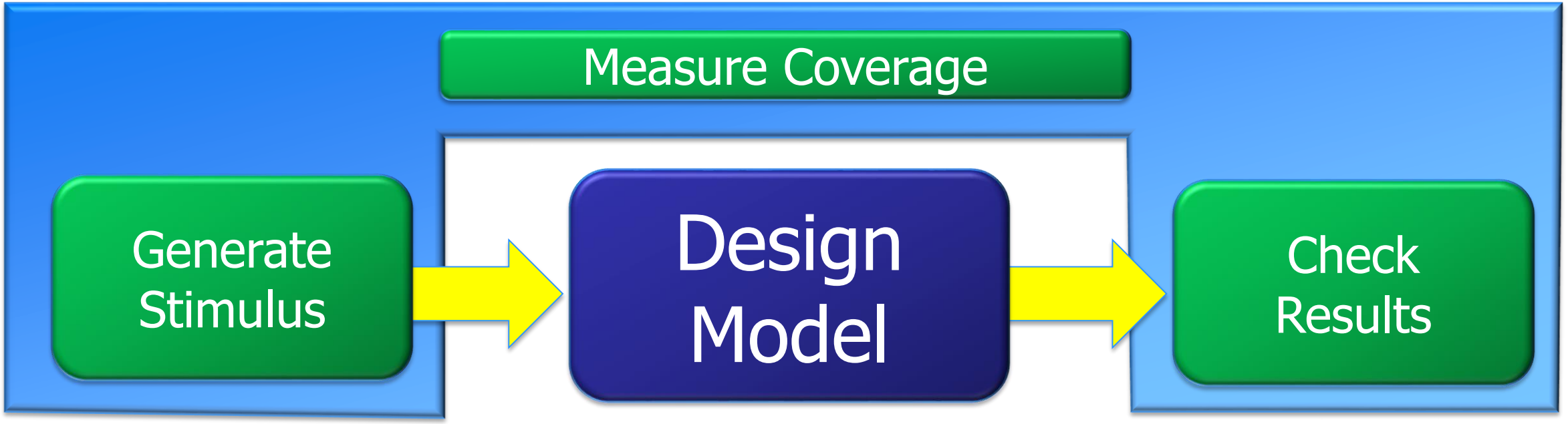
Directed-test-based simulation finds the bugs you can think of…

Constrained-random simulation finds the bugs you never anticipated!

VERIFICATION BEST PRACTICES

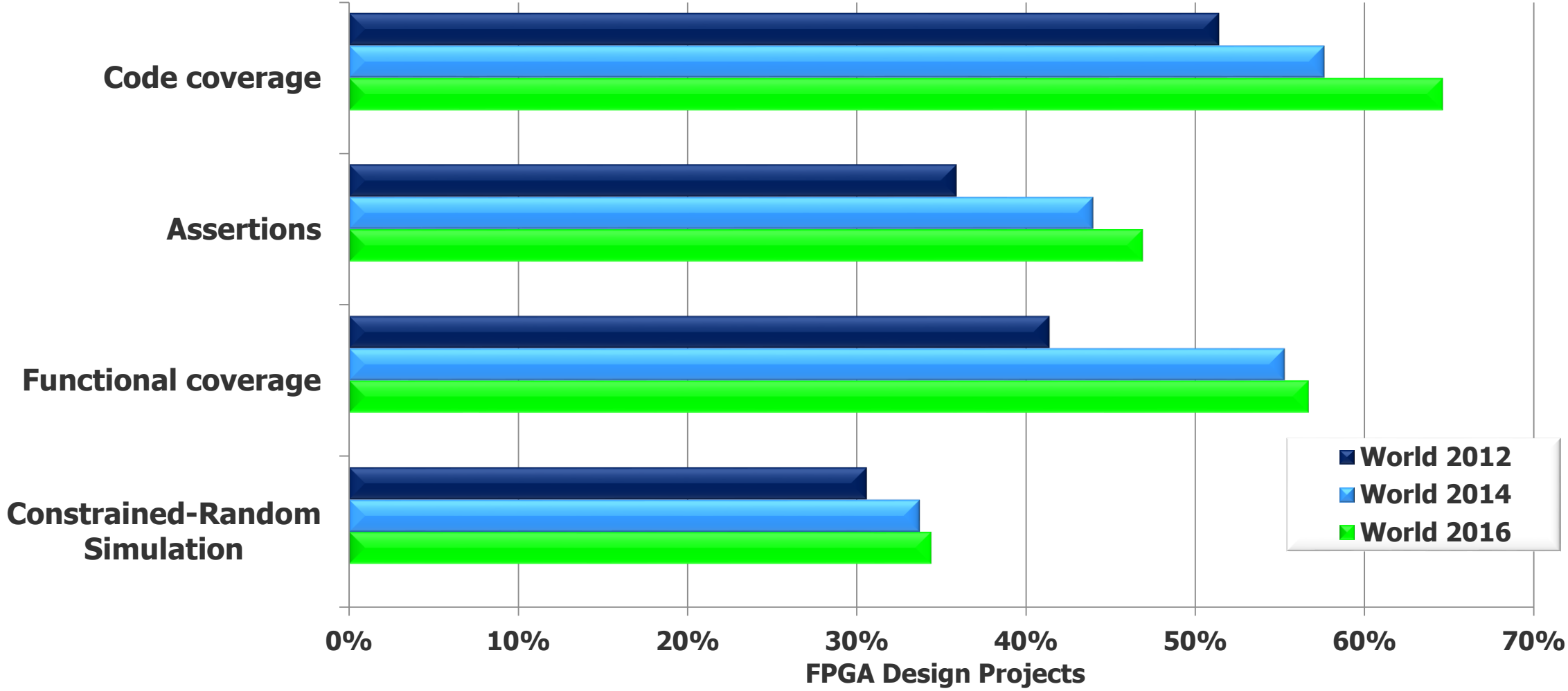
Simulation-Based Techniques

- Fundamental verification technique in use today
- Generally scales well
- Testing all possible states is generally incomplete



Assertions can be used to check results and measure coverage

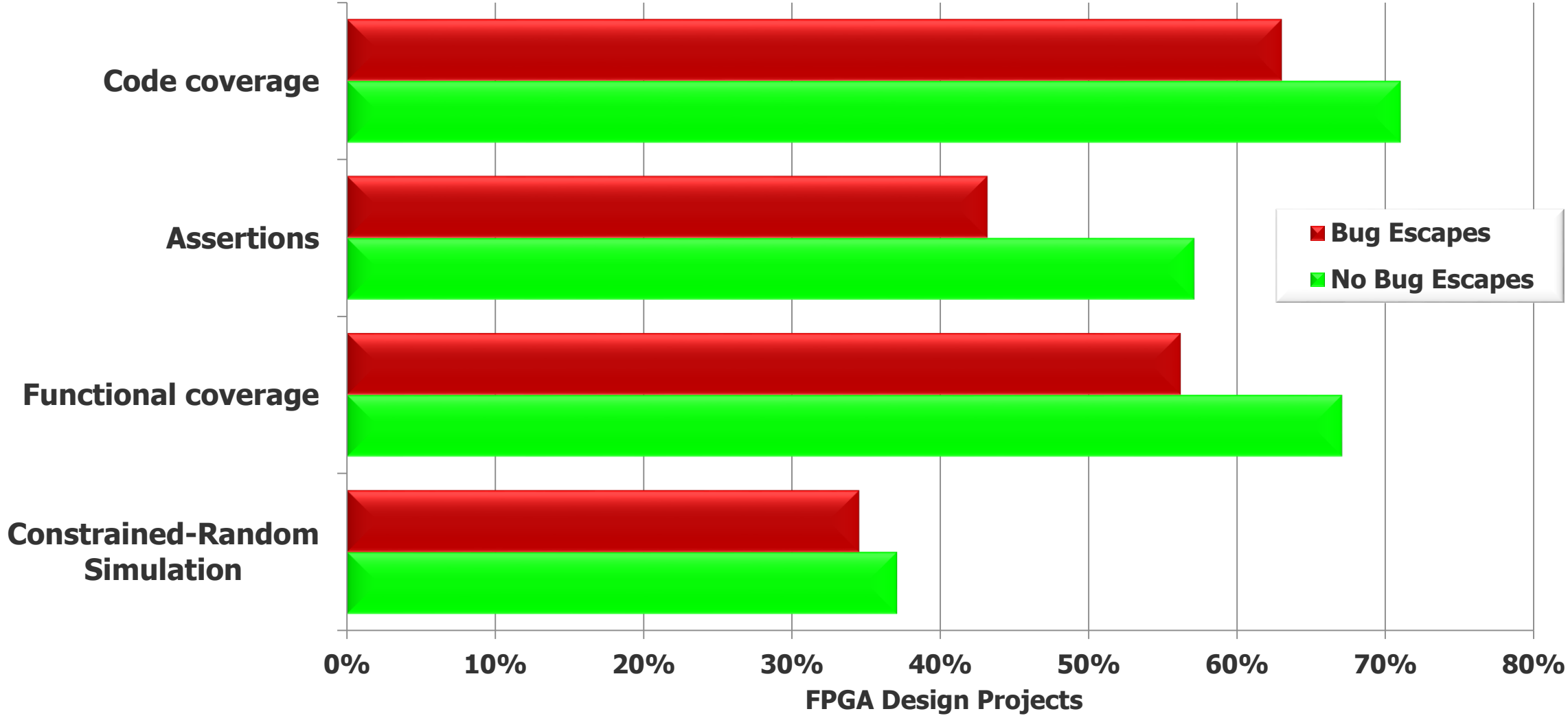
FPGA Projects are Maturing their Verification Processes



Source: Wilson Research Group and Mentor Graphics, 2016 Functional Verification Study

FPGA Verification Technology Adoption and Bug Escapes

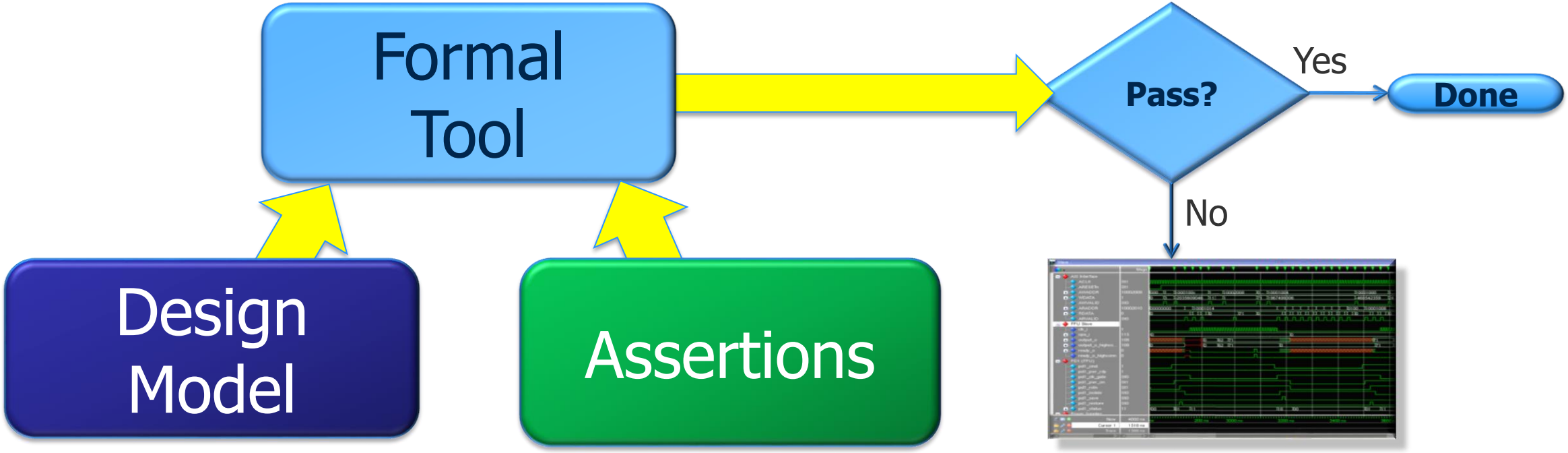
Data suggest organizations that are less mature in their verification processes experience more bugs



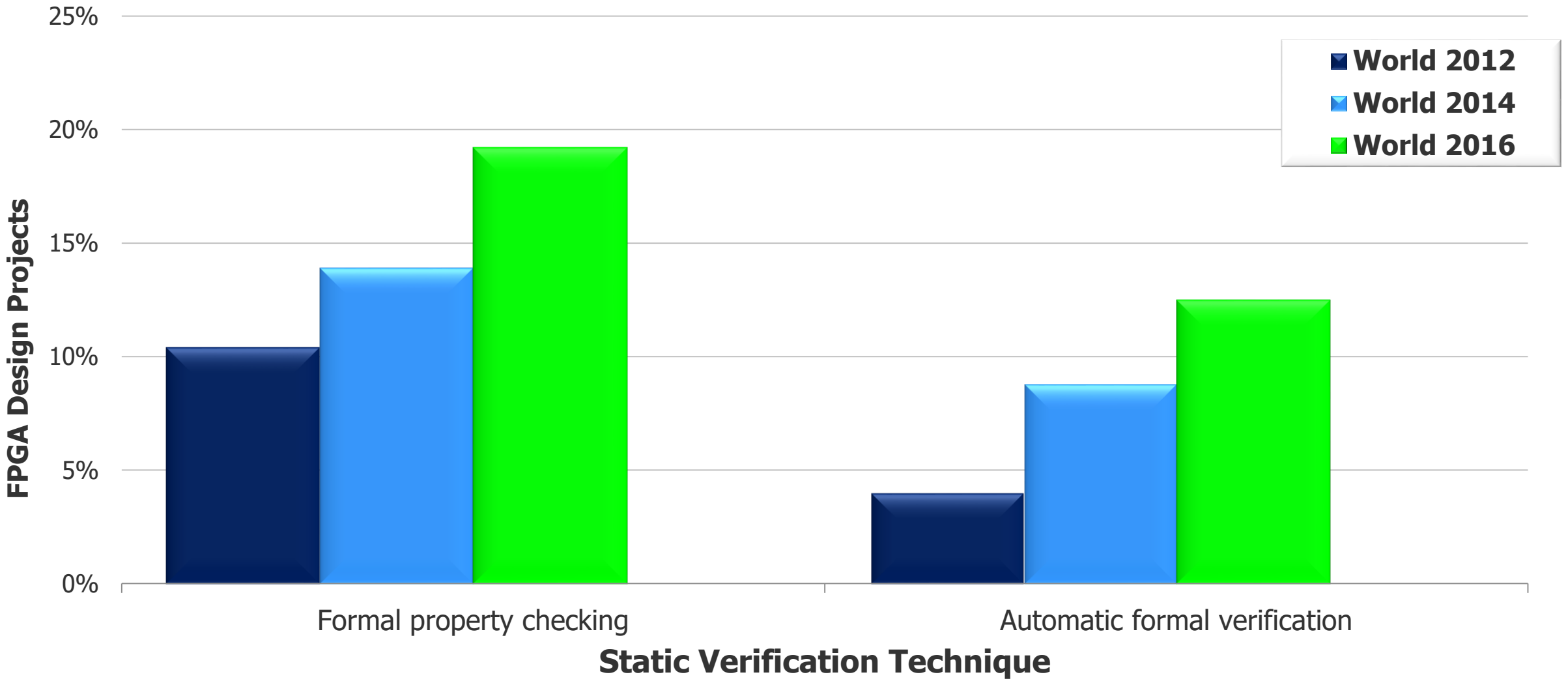
Source: Wilson Research Group and Mentor Graphics, 2016 Functional Verification Study

Formal-Based Techniques

- Does not require a testbench or input stimulus!
- Automatically uses algorithms to verify the functionality
- Verification can be complete
- Complements simulation-based techniques



FPGA Formal Technology Adoption Trends



Source: Wilson Research Group and Mentor Graphics, 2016 Functional Verification Study

Proven Benefits from Advanced Verification

FPGA customers realize the benefits of evolving their verification methodologies

SystemVerilog

- Constrained random for better testing
- Functional coverage for better insight
- Assertions to improve debug efficiency

UVM

- Enables benefits of SystemVerilog
- Provides consistent methodology
- Promotes reuse for productivity boost

Verification IP

- Protocol expertise
- Reduces TB development effort
- Risk reduction

FPGA Customer Success Stories

- Increased business due to shorter design cycles
- 400% ROI after adopting UVM and VIP
- 5 straight FPGA's without a bug
- Zero bugs found in lab since moving to UVM
- Reduced expensive lab equipment
- 100x faster to debug vs lab

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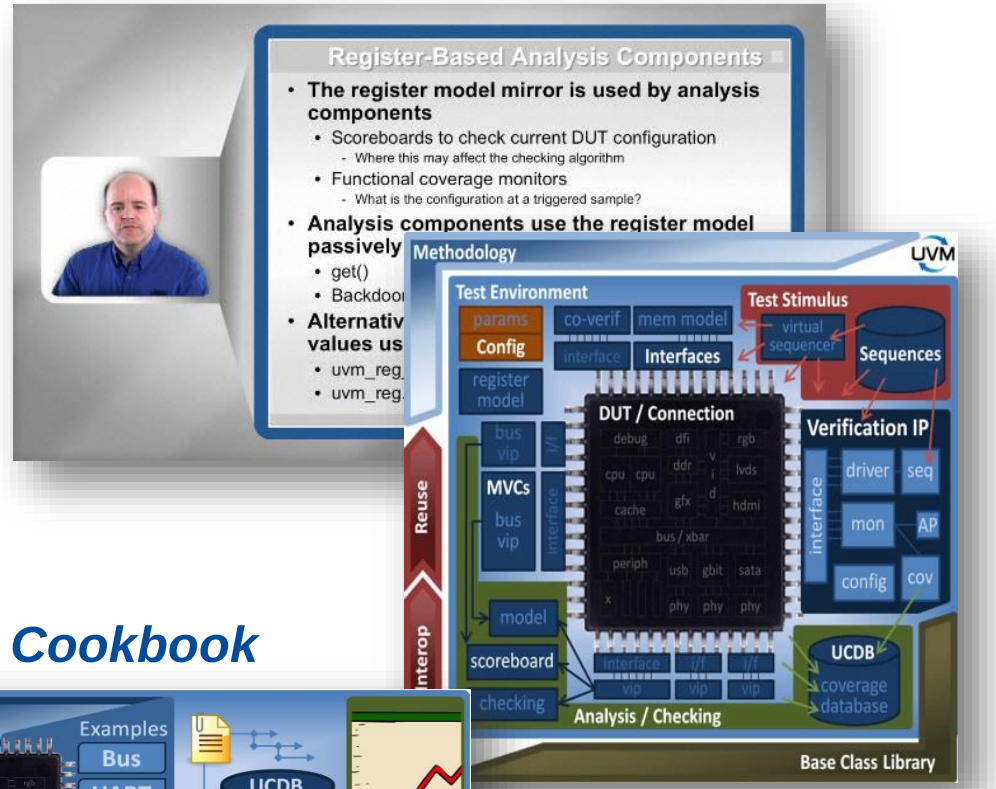
IMPROVING VERIFICATION SKILLS

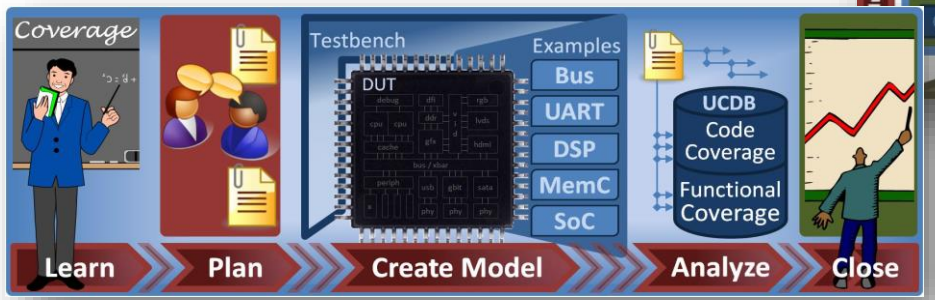
The Most Comprehensive Verification Resource Around

Free Resource Available to You!

- Online Courses
- Verification Cookbooks
- Discussion Forums
- Patterns Library



Coverage Cookbook



UVM Cookbook

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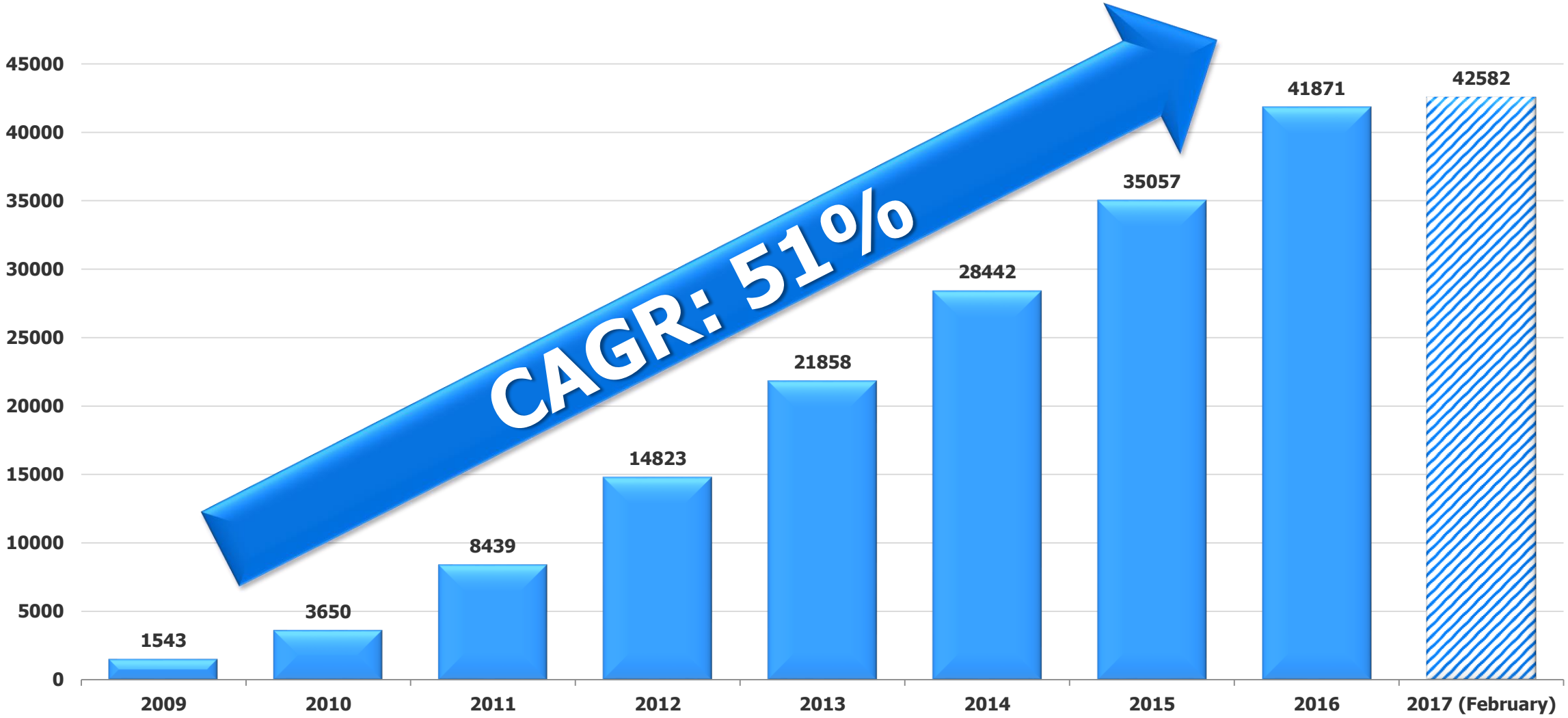
Verification Academy Membership Trend

Free Resource Available to You!



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Learn More About Mentor's FPGA Design & Verification Tools and Solutions

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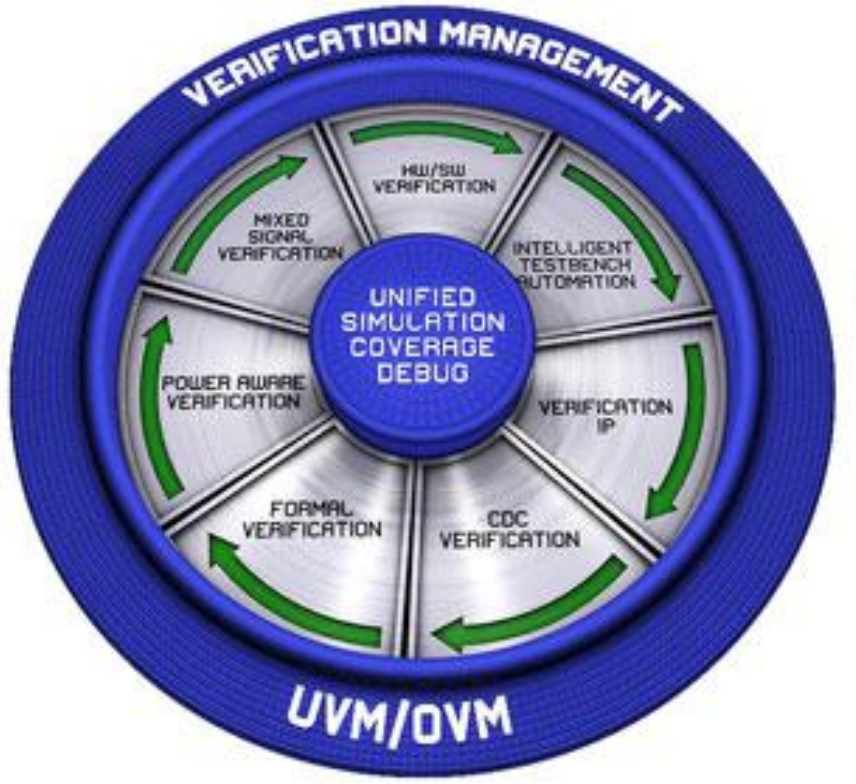

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