IPU – A Paradigm Shift in Infrastructure Processing

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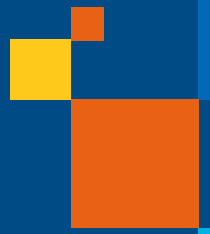

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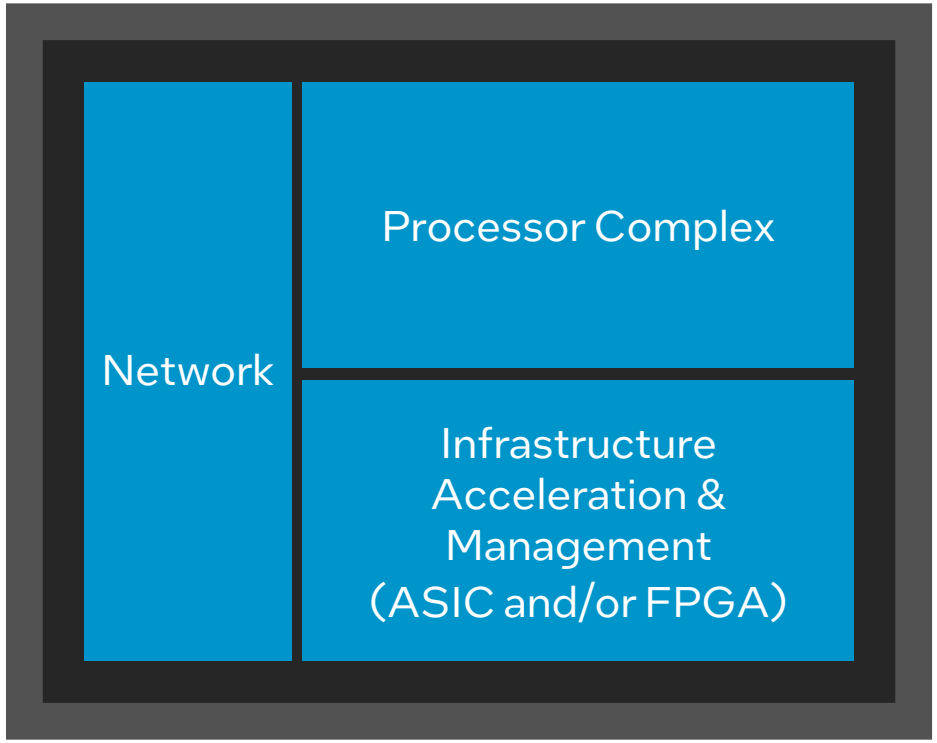
Intel® Infrastructure Processing Unit (IPU)

Providing new data center value



- Highly intelligent **infrastructure acceleration**
- System-level **security, control, and isolation**
- **Common** software frameworks
- HW and SW **programmable**, built to customer needs

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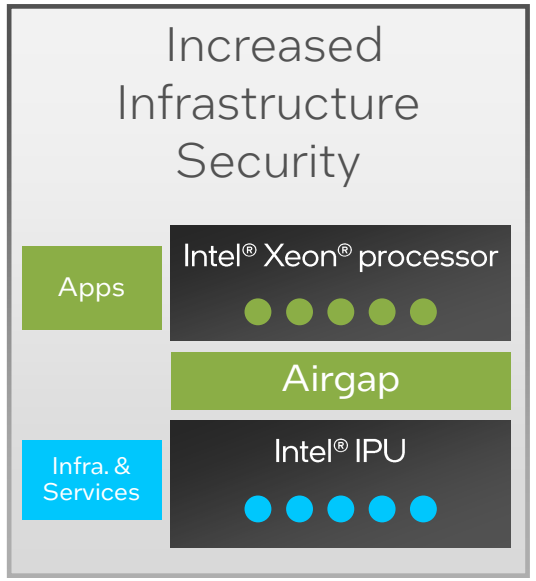
Processor complex enables control plane offload and isolation

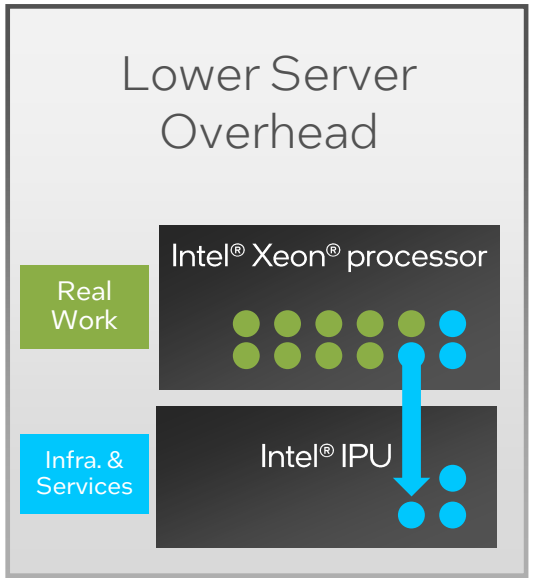
Intel® IPU Value Proposition

Security



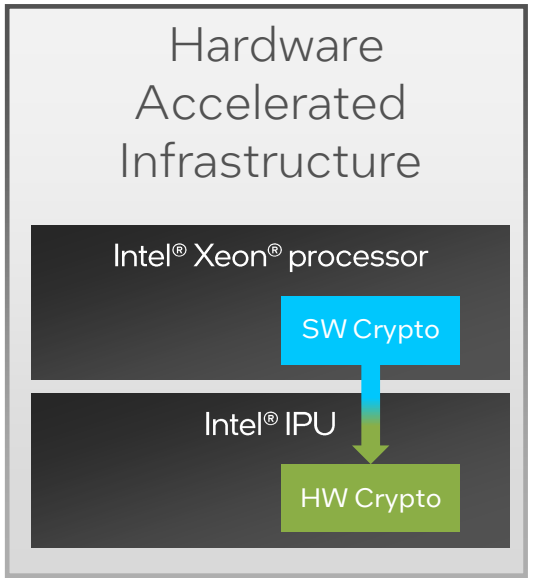
Application & Tenant Isolation from Infrastructure

Infrastructure Offload



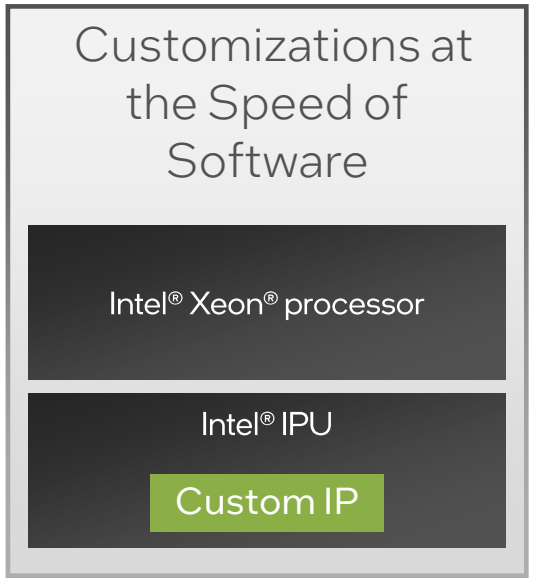
IPUs Reduce Host Compute Cycles Doing Infrastructure Work

Infrastructure Acceleration



IPUs Can Accelerate Some Applications

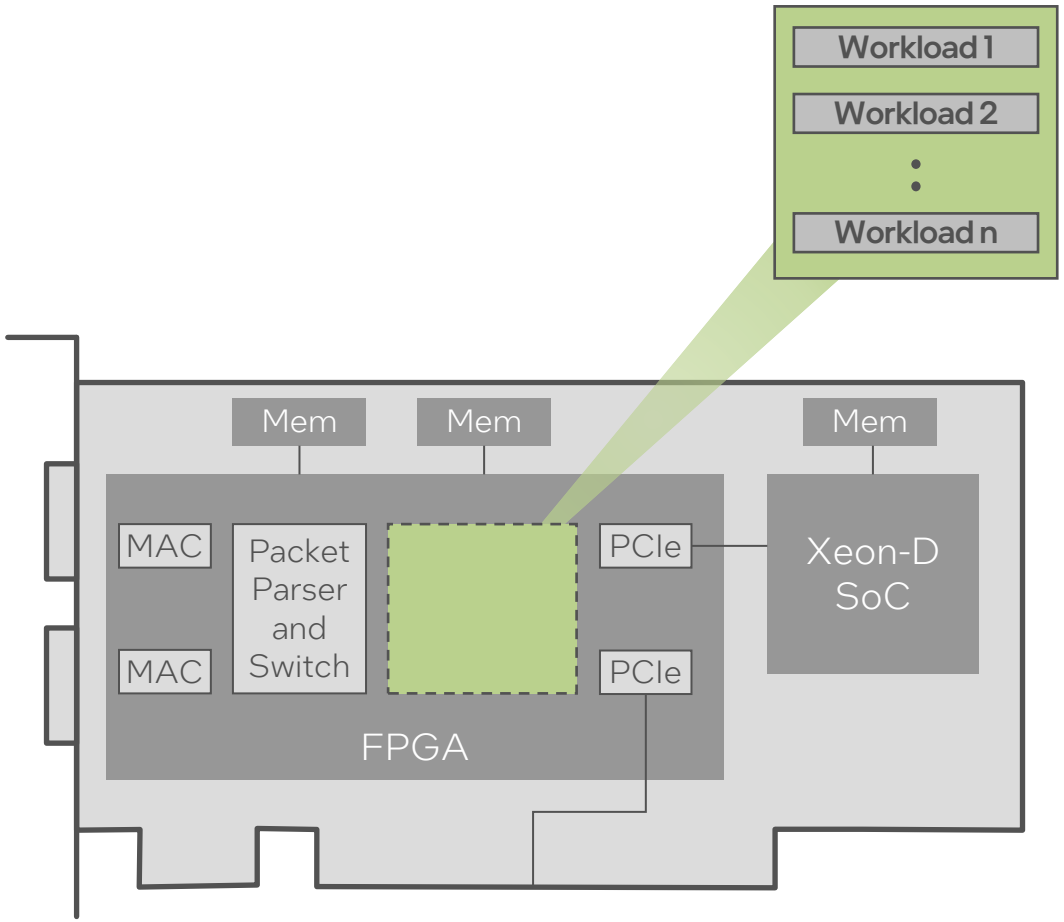
Feature Velocity



IPUs Provide Reconfigurability and Programmability

Isolation of workload and infrastructure improves integrity and efficiency of the grid

Acceleration Workloads



Protocols
- TCP/IP, RoCEv2, VxLAN, Geneve, NVGRE

Network Switching/Routing
- Data plane: OvS, P4
- Analytics: Network Analytics (AI)

Security
- Encryption: TLS, KTLS, IPSec, MACSec
- Firewall → ACLs
- DDoS Mitigation

Storage
- NVMe Tunnel, NVMe-oF TCP, NVMe-oF RoCEv2, Erasure Coding, Compression

AI/ML
- ML → LSTM

Big Data
- Arrow/Arrow Flight

One Platform, Multiple Workloads

Intel® IPU Roadmap

Open Community

DPDK SPDK P4 ipdk Infrastructure Programmer Development Kit OPEN PROGRAMMABLE INFRASTRUCTURE PROJECT

Open SW Ecosystem

Broad Adoption Enabled by Leading and Expanding Ecosystem

Serving Cloud, CoSP, Enterprise and Beyond

Leadership Portfolio

2022 — Today

2nd Gen 200G

FPGA+IA platform **F2000X-PL**

ASIC **E2000**

2023/2024 — Announced

3rd Gen 400G

intel IPU

FPGA+IA platform Codenamed **Hot Springs Canyon**

ASIC Codenamed **Mount Morgan**

2025+ — Next Gen

4th Gen 800G

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FPGA+IA platform **Next Gen**

ASIC **Next Gen**

Multi-generation IPU with open ecosystem