



ÜberNIC: The Future of Networking. Today.

FPGA-Based Network Controller & Hardware Network Stack

Pure Performance | Unmatched Economics | Future Compatible

April 4, 2023



ÜberNIC It's Not Complicated

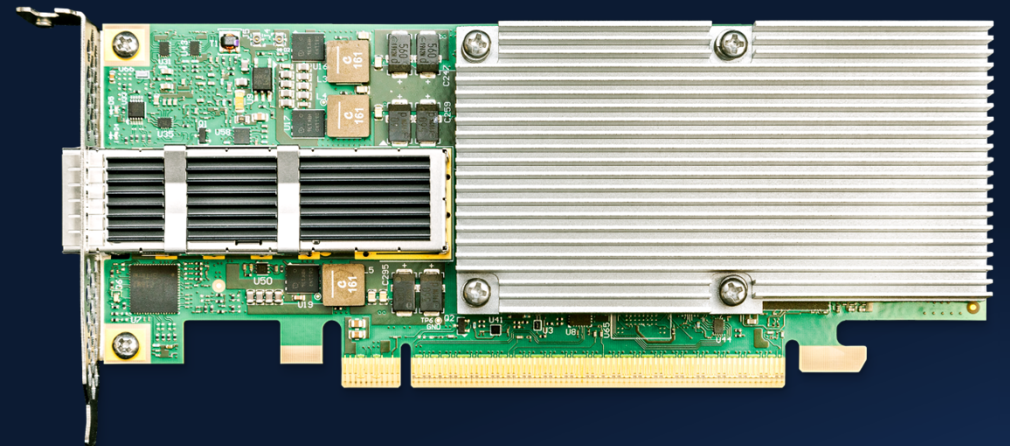


You don't need
a racing license
to drive a car...



You don't need
a PhD to fly a
jet plane...

...and you don't need to write a
single line of HLS, HDL, or RTL
to benefit from an FPGA chip...
you just need ÜberNIC...





ÜberNIC Industry-Leading Foundation



100% FPGA-Based Network Stack (i.e. 100% Offload)



Compliant w/RFC & IEEE Standards



Significant Fiber Density; Max 16 FPs








Multi-GB On-Board Memory; Max 64GB



Single Slot, HH ½ Length or FH ¾ Length

ÜberNIC Unmatched Performance & Usability

-  61% Lower Latency; Full RTT <558ns
-  267% Higher Throughput w/o Performance Loss
-  Highly Consistent; 95th Percentile Latency StDev 2.19%
-  Equally Supports PCIe 3.0, 4.0, 5.0 & CXL 1.1, 2.0
-  Plug & Play x86 I/O (BSD/POSIX; Raw Frame; Custom API)

Not a STAC Benchmark



ÜberNIC Empowers Extensibility



MAC-Based Timestamping



Market Data Handling & Line Arbitrage



Data Preprocessing, Filtering, & Enhancement



MAC-Based PCAP & Port Spanning



Simultaneous Network I/O Support for SW & HW EUC



ÜberNIC Supports Compute Express Link (“CXL”)

About CXL



Coherent Interconnect
Protocol Leveraging PCIe
Physical & Data Layers



Tightly Coupled Interaction
Creates Vastly Improved
Performance



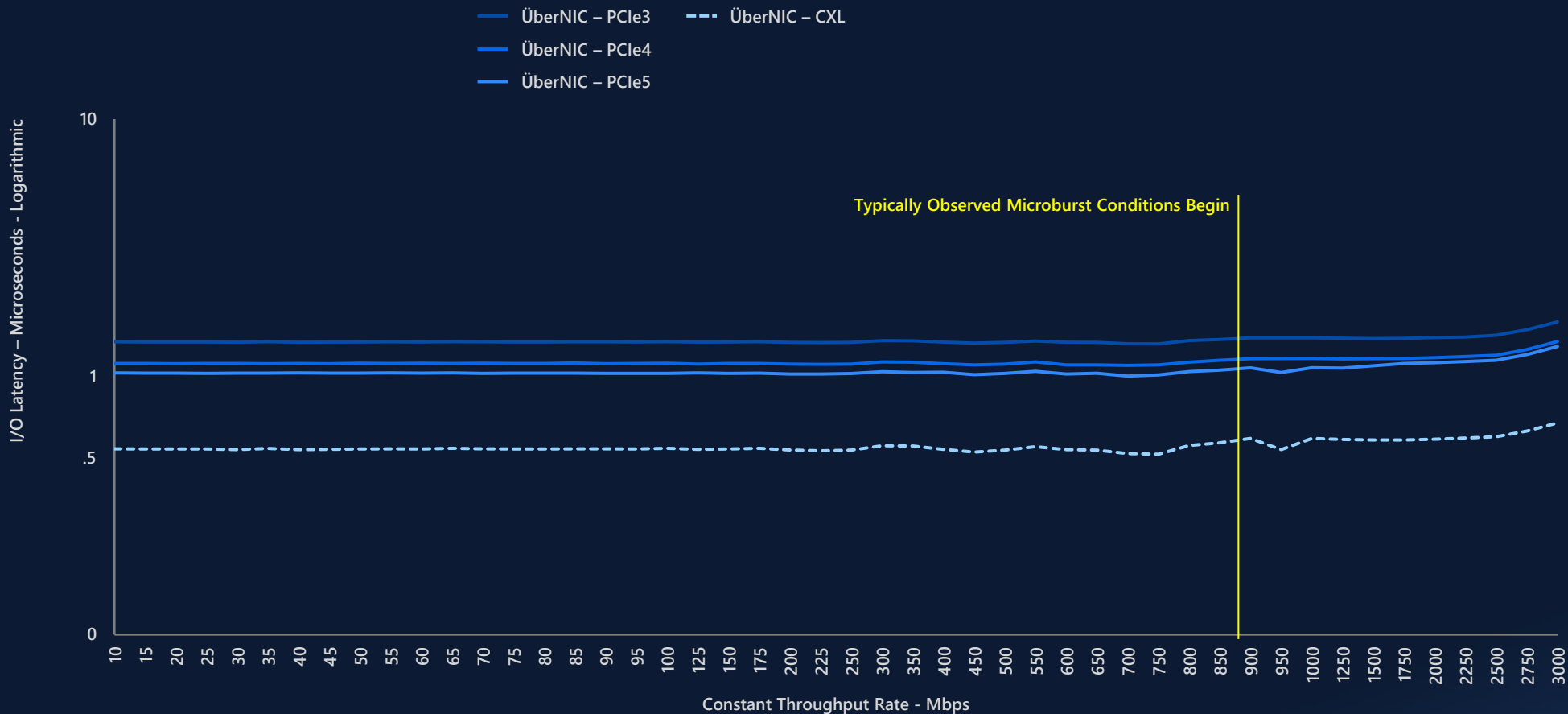
Enables Common Shared
Cache/Memory Between CPU
& Peripherals



1. CXL.io/CXL.cache
2. CXL.io/CXL.cache/CXL.mem
3. CXL.io/CXL.mem



ÜberNIC w/CXL 95th Percentile RTT Performance Summary

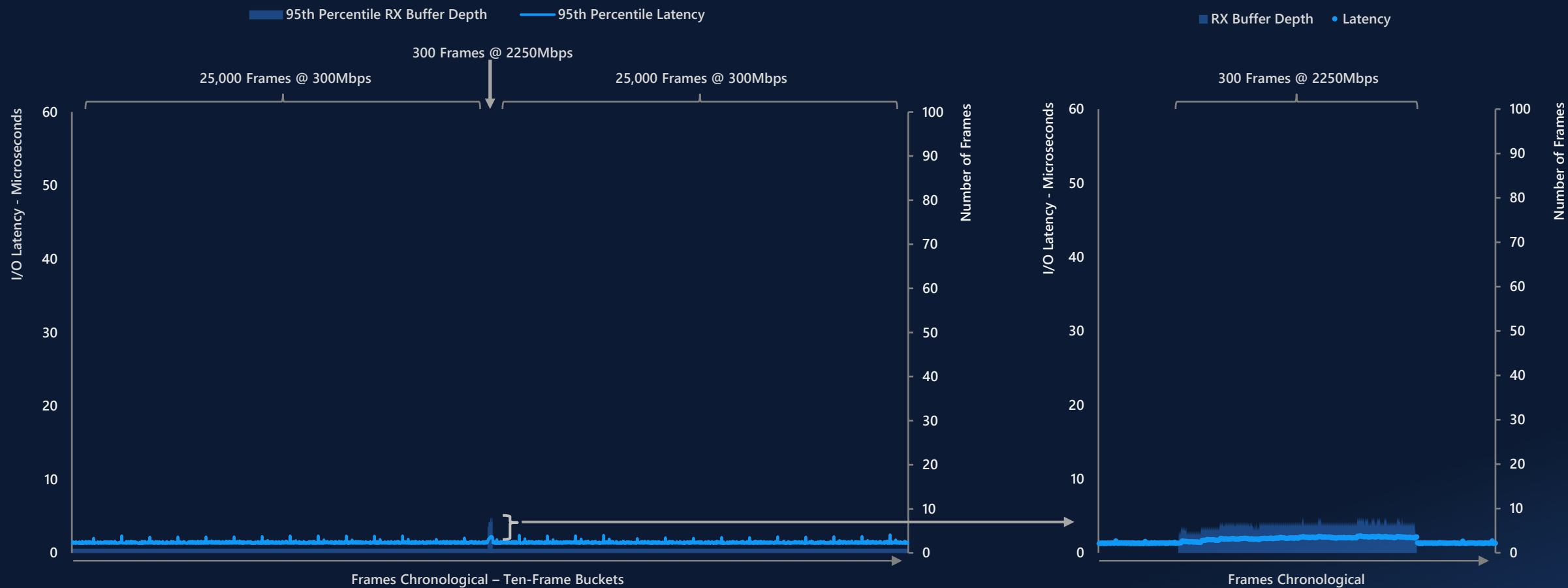


(ÜberNIC Tested Using Pre-Production Intel® Agilex™ 7 I-Series & Non-Optimized Code)

Tested By Naros.TaSR Not a STAC Benchmark

50,000 Frames Per Throughput Rate | 10GbE | 64B UDP Payload (110B Frame) | Transceiver to Transceiver L2 SOF to SOF via Linux User-Space | Excluding Business Logic

ÜberNIC Microburst Handling – RTT via PCIe3



(ÜberNIC Tested Using Pre-Production Intel® Agilex™ 7 I-Series & Non-Optimized Code)

Tested By Naros.TaSR Not a STAC Benchmark

50,300 Frames | Multi-Step Variable Throughput Rate Run | 10GbE | 64B UDP Payload (110B Frame) | Transceiver to Transceiver L2 SOF to SOF via Linux User-Space | Excluding Business Logic



ÜberNIC Designed For Performance & Efficiency

ÜberNIC Ultra Wide & Ultra+ Wide

2x QSFP-DD
Max 16 FPs

Aux Power Socket

Socketed DDR4
Max 64GB

PPS In

Intel® Agilex™ 7 FPGA
AGI019 or AGI023

ÜberNIC Ultra & Ultra+

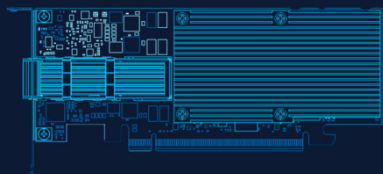
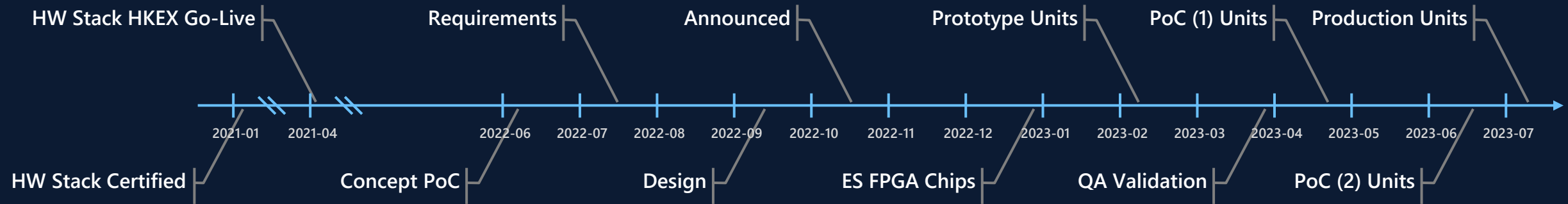
1x QSFP-DD
Max 8 FPs

Soldered DDR4
16GB

16 Lanes
PCIe 3, 4, 5; CXL 1.1, 2.0



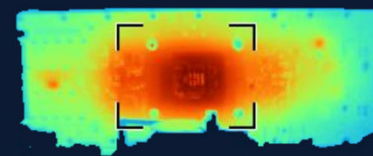
ÜberNIC Concept to Deployment



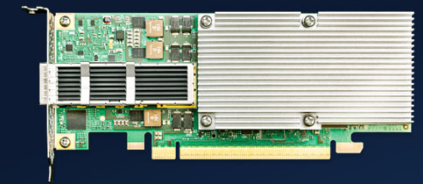
Design



Prototype



Testing



Production



Where Other Vendors Have Questions, Roadmaps, or Misplaced Claims...

...LMS & Intel Have Solutions



ÜberNIC Solves Your Data Latency & Ingestion Problems

Sample Boards Available Q2 2023



Lets.Talk@liquid-markets.com

CH: +41-79-877-6185 | US: +1-212-784-6145 | JP: +81-50-5539-9608