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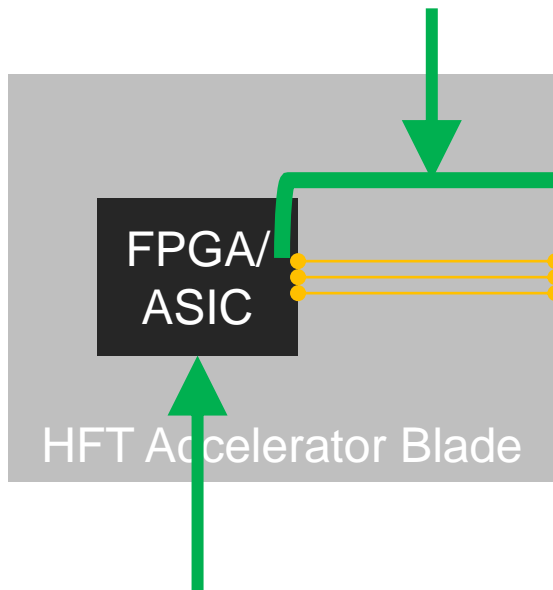
# The Edge of the Edge: PCB Latency in Trading Reaction Time

May 2023

# The Edge of the Edge: Extracting PCB Latency from Reaction Time

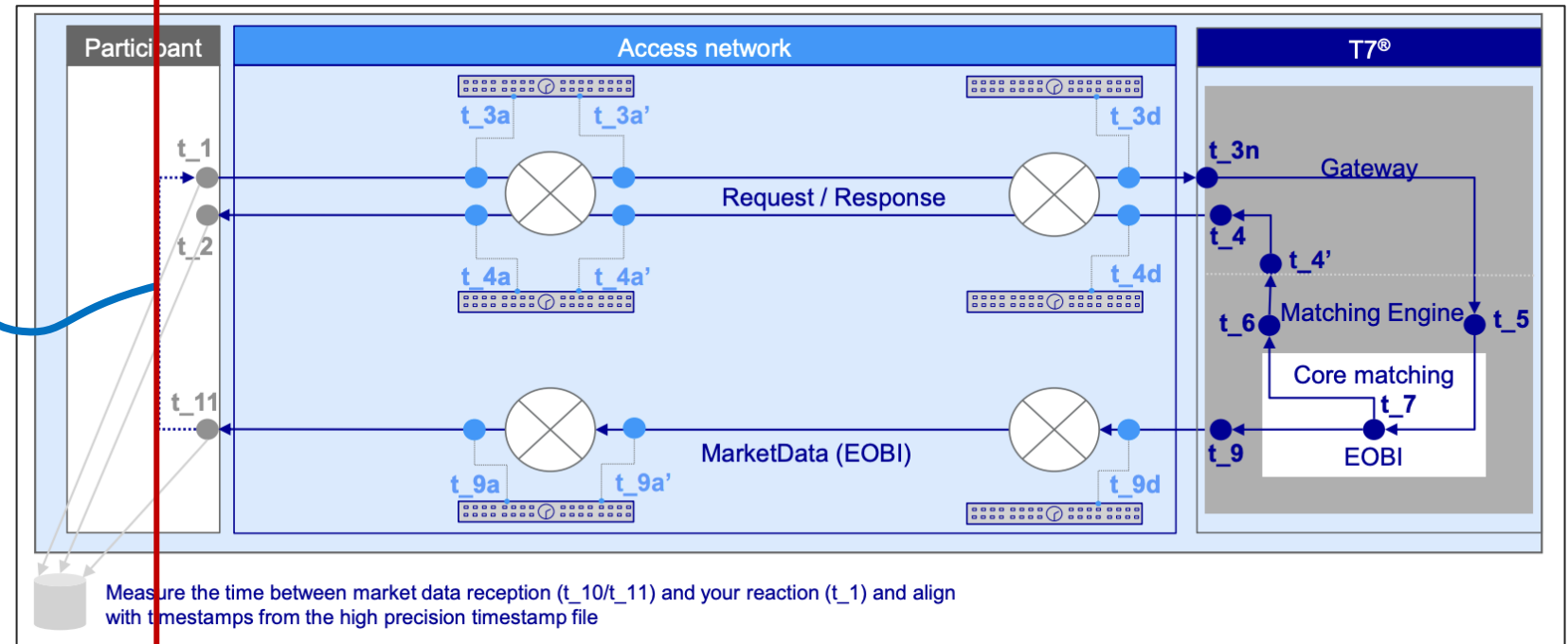
## Edge of the Edge

New focus area now that fastest vs mainstream reaction team is < 100ns



Existing edge computing to reduce reaction time

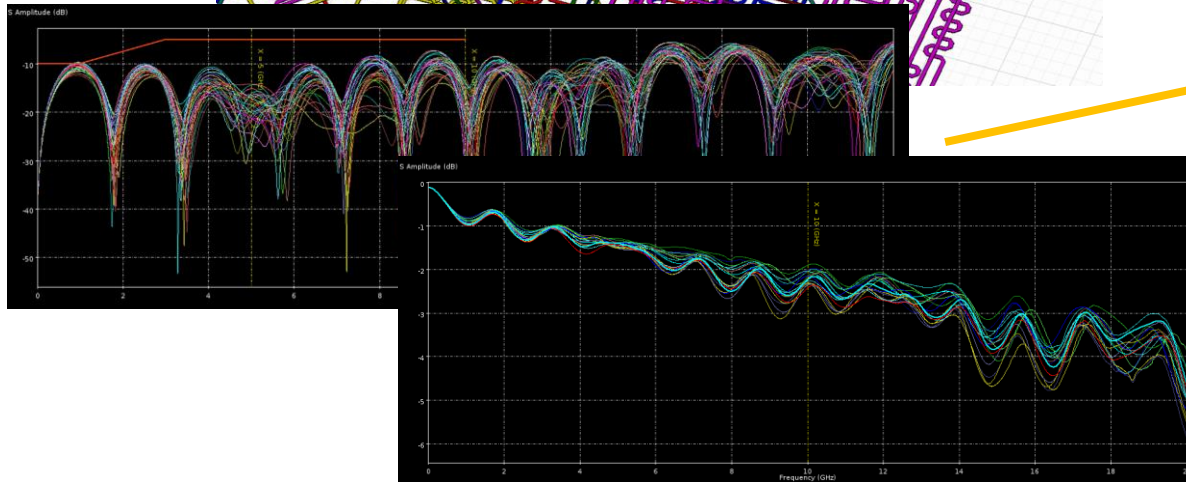
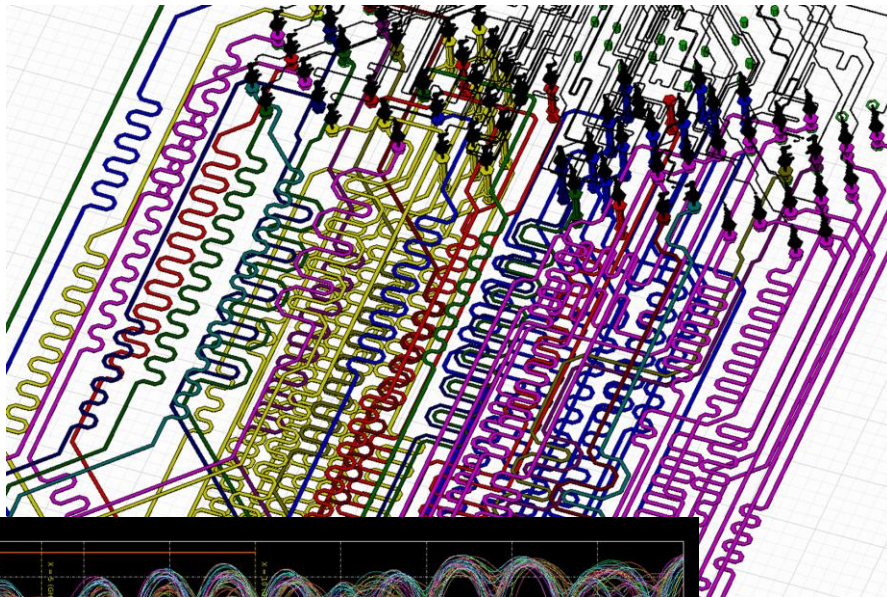
Fixed/Commercial latency: switches, networks



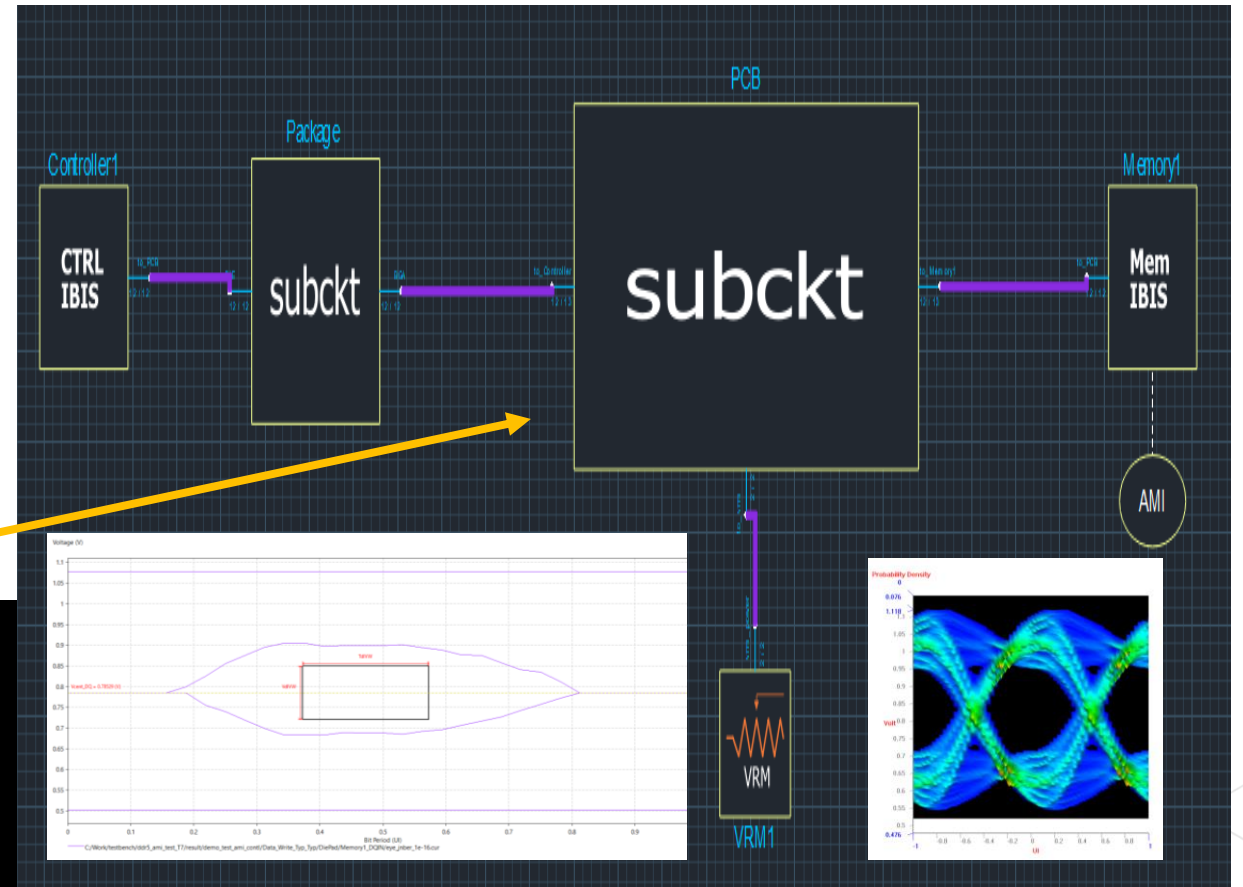
Source: Insights into Trading System Dynamics, Deutsche Börse Group, July 2021

# Cadence MSA/PCB Solution

- Full Wave 3D Extraction with Clarity

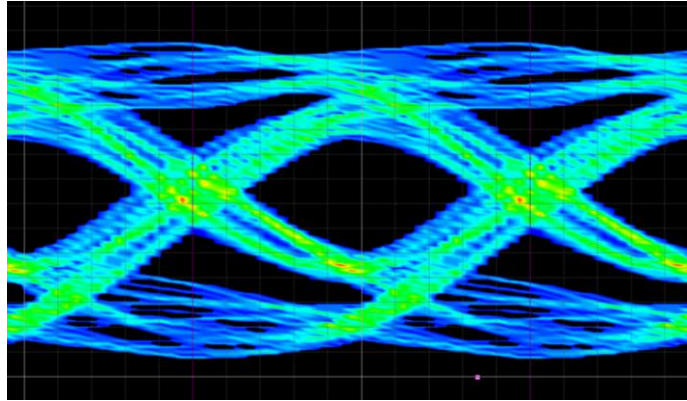


- Time Domain Simulation / Compliance Verification with SystemSI



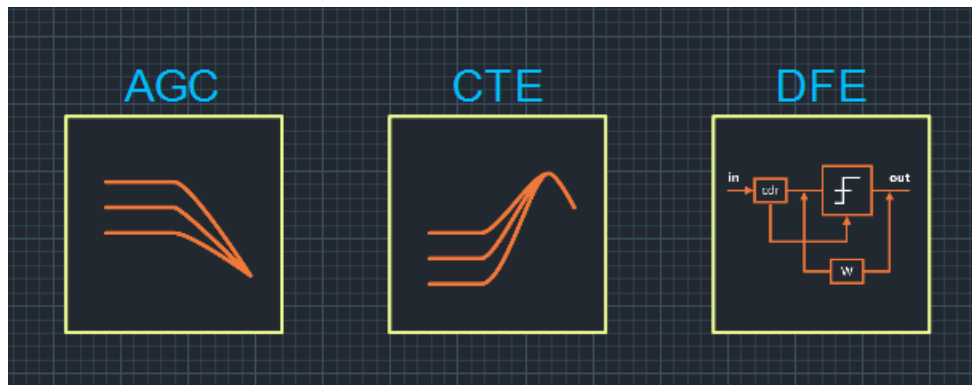
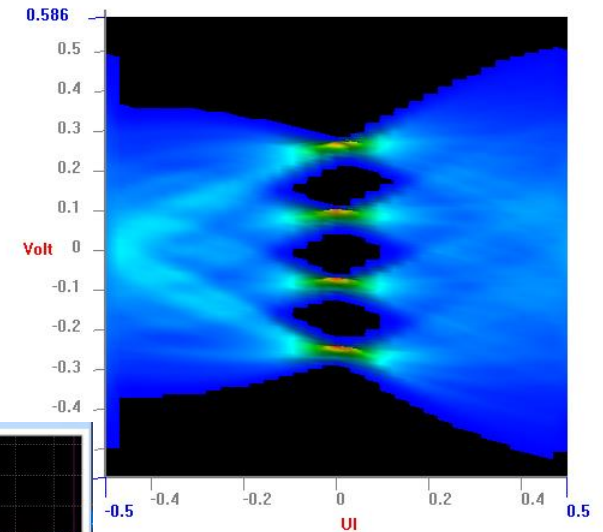
# Innovations in High Speed Bus Design

- Signal integrity is crucial
- Advanced equalization enabling major high speed data throughput
- Pulse Amplitude Modulation (PAM) signaling allows multiple bits per transmitted symbol

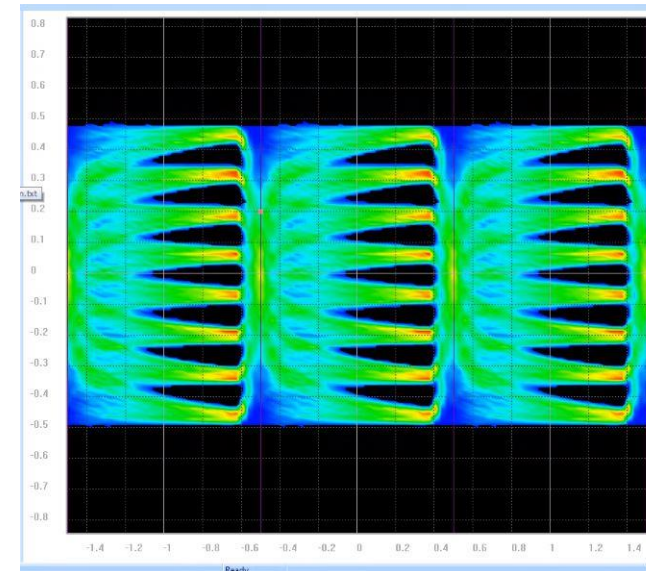


“PAM2” @ 16Gbps (GDDR6)

112Gbps PAM4 Signaling



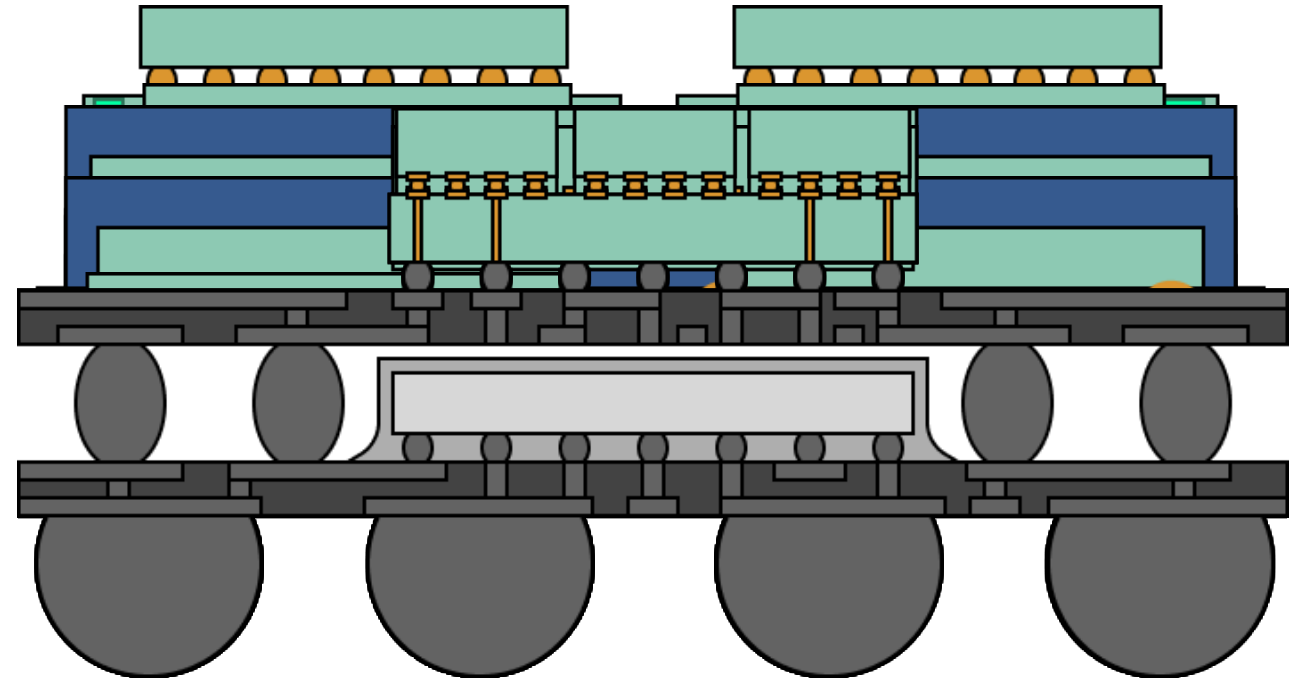
Advanced Equalization



PAM8 Signaling

# Packaging Technology for Low Latency

- New packaging techniques reduce physical form factor, and associated interconnect delays
- Combinations of interposer, advanced package, and printed circuit board (PCB) technology are being rapidly adopted



# Cadence: HFT Accelerator Partner

Contact us:  
hft@cadence.com

## Digital Design to Implementation

High Level Synthesis  
Physical RTL Synthesis

Place and Route

Liberate™

Tempus™

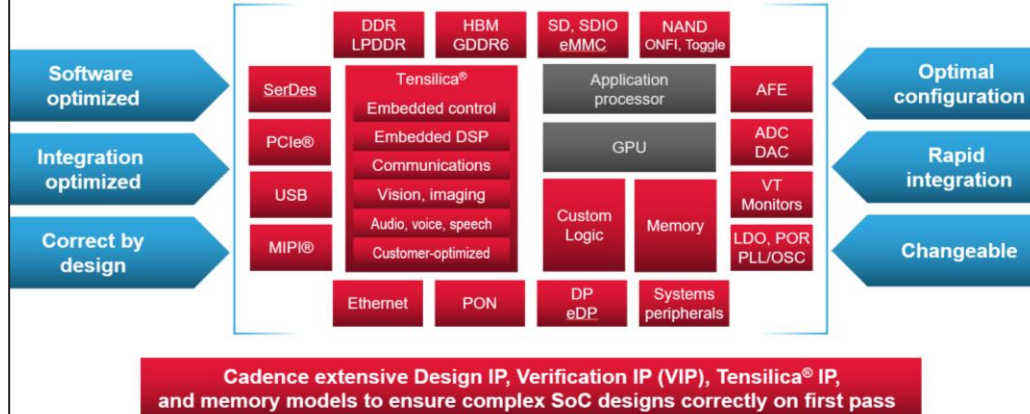
Voltus™

Pegasus™

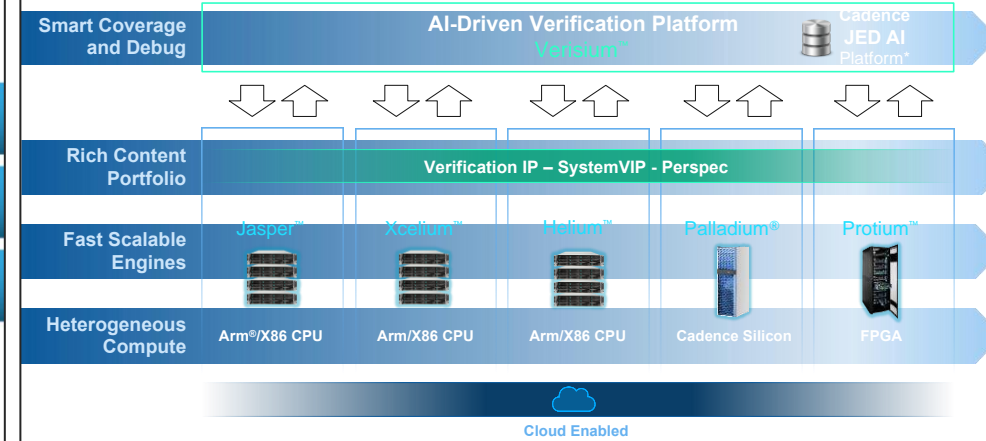
Quantus™

## Cadence IP Solutions

Silicon-proven in advanced nodes

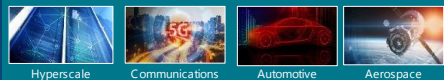


## Cadence Verification Full Flow



## Next-Generation SI/PI

Sigrity X delivers up to 10X performance on large-scale system analysis



Tightly integrated, leading SI/PI technology across Cadence design platforms

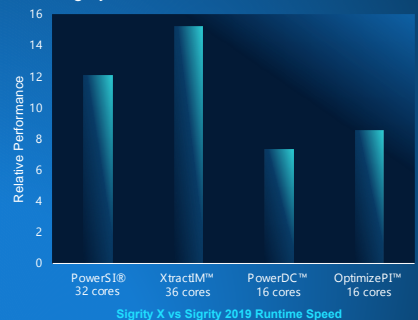
Enables PCB and IC package designers to incorporate end-to-end, multi-fabric, multi-board systems (from transmitter to receiver or power source to power sink) for Signal Integrity / Power Integrity signoff success

System Analysis and Signoff



Allegro® PCB & IC Package design tools

Sigrity™ X Runtime Performance Gain



- ASIC solution: Broadly adopted in high-speed comms and mission-critical applications
- High-performance IP: Proven in leading comms systems
- Tensilica® IP: Proven processor technology used in autonomous drive and other high-reliability apps
- Verification solution: Apply objective analysis to improve FPGA and prepare for ASIC
- High-speed PCB: Integrated Multiphysics Systems Analysis (SI/PI/Thermal)
- Services: Expert RTL to GDS design services



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