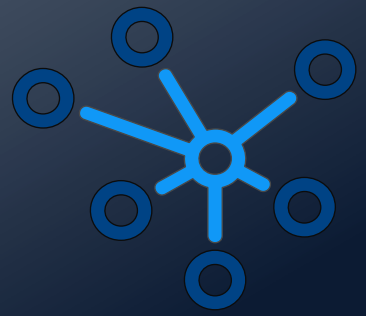

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LIQUID-MARKETS SOLUTIONS

THE POWER OF THE POSSIBLE™

ÜberNIC™

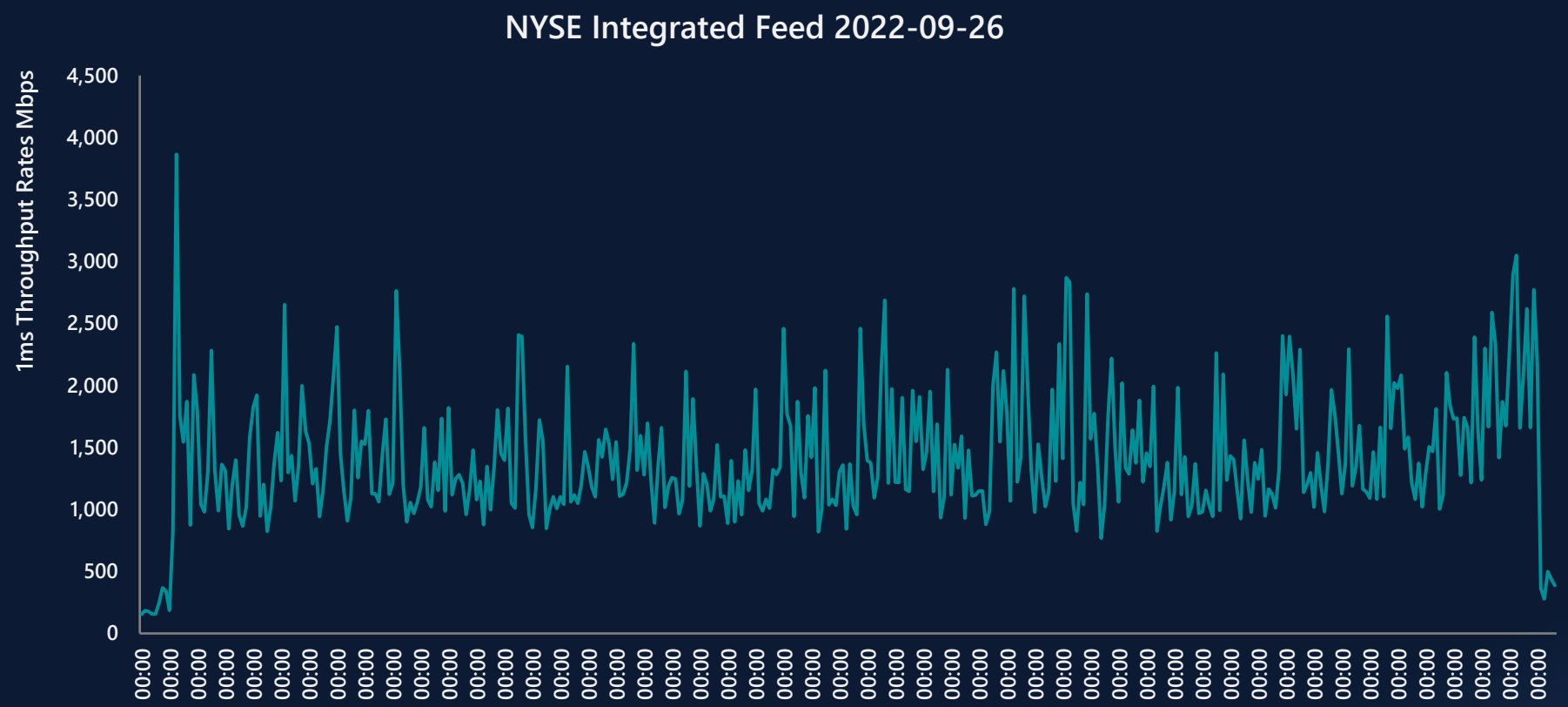
Your NIC Can't Keep Up With Modern Markets – Ours Can

November 30th, 2022

73.2%

Market Data Messages w/Payloads <= 100 Bytes

The Real World: Frequent Exchange Microbursts



Source: https://marketdatapeaks.net/

Can Your NIC & Network Stack Handle Real World Scenarios?

Why The $#!&%$ Are My Orders Not Done?

The Solution: ÜberNIC™

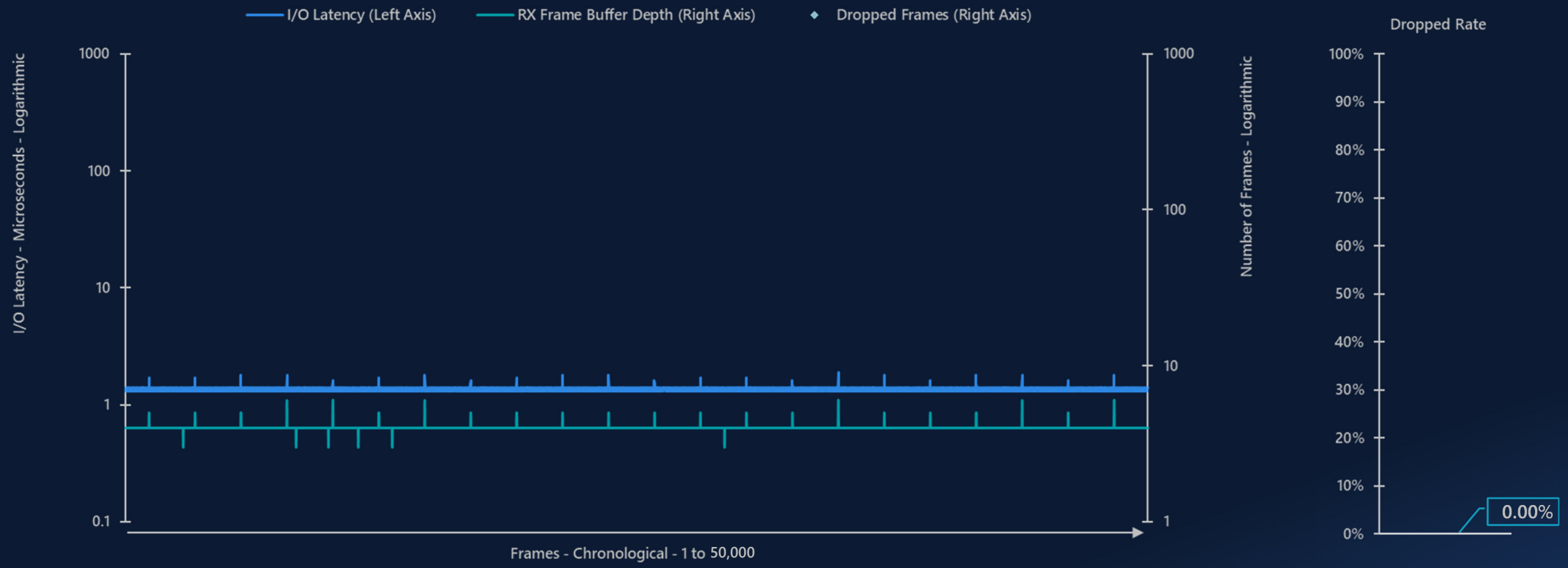
Summary: ÜberNIC™

- Performance
  - FPGA-Based NIC Implementing a 100% Hardware Network Stack
  - On-Board Memory Enables Highly Performant & Lossless Buffer
  - Ultra-Low-Latency & Ultra-High-Throughput in a Single Package
  - Sockets-Compliant, Highly-Optimized PCIe Transfer and Kernel Bypass
- Standards Adherence
  - Fully Integrated with Linux Tools (IP, IFCONFIG, ETHTOOL)
  - End-User Configuration Preferences (ex: Congestion Control, Retransmit)
  - Fully Transparent Disclosure & Documentation
- Extensible
  - Timestamping (NTP, PTP, PTP + PPS, FPGA Clock-Counter)
  - Internal PCAP
  - Market Data Protocol Handler(s)

Extremely Deterministic, Ultra-Low-Latency & Ultra-High-Capacity

The Real World: Meet ÜberNIC™...

ÜberNIC™ Ultra (PCIe Gen 3) @2000Mbps (*Pre-Production Silicon & Non-Optimized* Code)



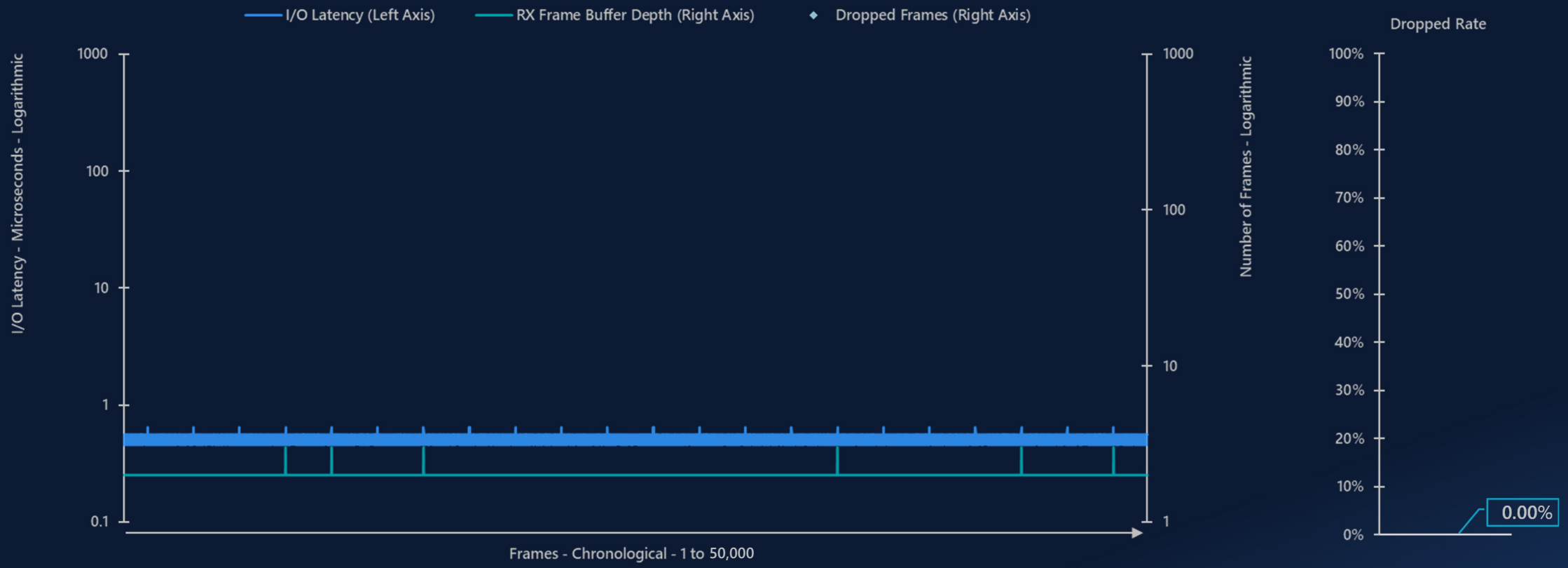
Not a STAC Research Benchmark

Pre-Production Intel Agilex I-Series Tested By Naros.TaSR™

50,000 Frames | 64B UDP Payload (110B Frame) | Transceiver to Transceiver L2 SOF to SOF via Linux User-Space | Excluding Business Logic

The Real World: Meet ÜberNIC™...

ÜberNIC™ Ultra (CXL) @2000Mbps Constant Rate (*Pre-Production Silicon & Non-Optimized Code)*



Not a STAC Research Benchmark

Pre-Production Intel Agilex I-Series Tested By Naros.TaSR™

50,000 Frames | 64B UDP Payload (110B Frame) | Transceiver to Transceiver L2 SOF to SOF via Linux User-Space | Excluding Business Logic

The Real World: Meet ÜberNIC™...

Performance Consistency (*Pre-Production Non-Optimized Code*)

Throughput - Mbps	ÜberNIC™ w/PCIe Gen 3 Latency StdDev	ÜberNIC™ w/PCIe Gen 3 Drop Rate	ÜberNIC™ w/CXL Latency StdDev	ÜberNIC™ w/CXL Drop Rate
600	24ns	-	13ns	-
750	21ns	-	12ns	-
800	24ns	-	13ns	-
825	24ns	-	14ns	-
900	23ns	-	14ns	-
1000	23ns	-	13ns	-
1250	25ns	-	16ns	-
1500	30ns	-	17ns	-
2000	37ns	-	21ns	-
2500	55ns	-	21ns	-
2750	76ns	-	30ns	-

Not a STAC Research Benchmark

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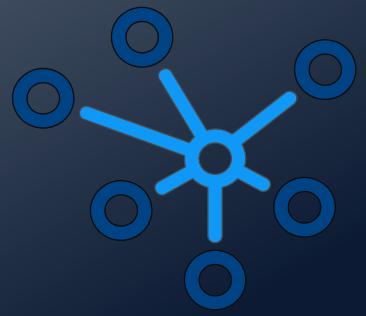
ÜberNIC™ Incorporates…

- Entire Network Stack in Hardware
- FPGA Board Designed For FSI
- CXL for Unimagined Performance



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Contact LMS or Your Intel Representative to Learn How ÜberNIC™ Solves Your Data Latency & Ingestion Problems

Pre-Production Sample Boards Available Q1 2023

Lets.Talk@liquid-markets.com

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