

STAC Summit - November 2022

What CXL means for FSI

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New CXL protocol
is game changing!!

Matt's prediction is coming
to fruition...



Dr. Matthew Grosvenor
at Global STAC Live
(Spring 2020)



Introduction



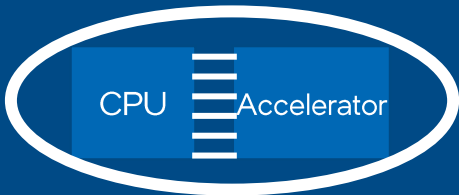
Application/Workload Acceleration
(Data transformation)

Infrastructure Acceleration
(Processing of data in motion)

Smart Storage/Memory
(Processing of data at rest)

Choose best accelerator HW: CPUs, GPUs, AI, FPGAs, other chipsets

CXL Improves Efficiency

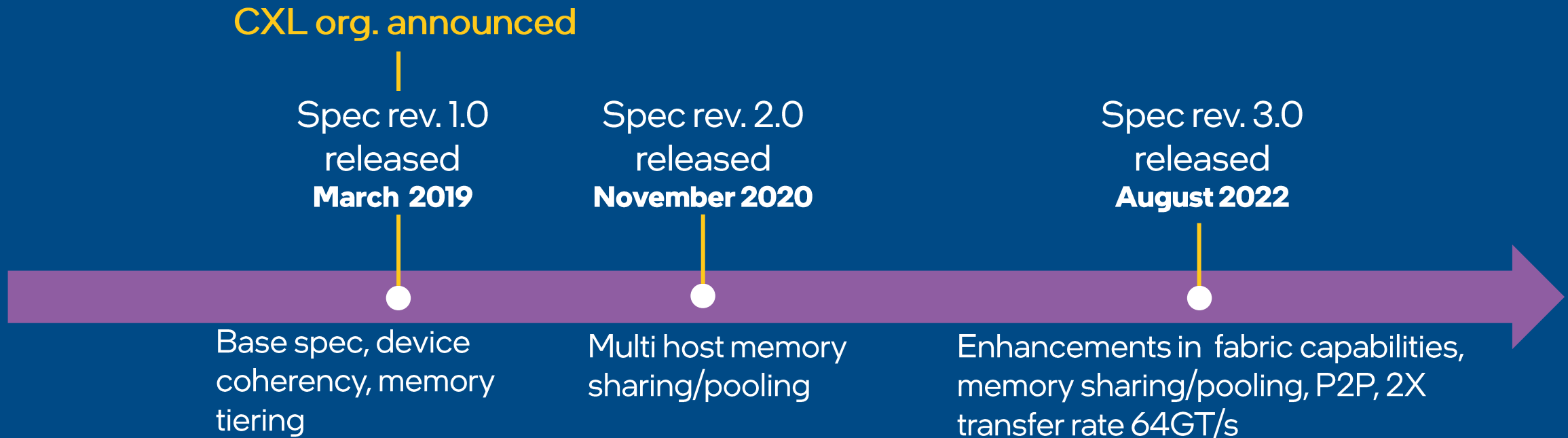


Close
Coupling

↙ Lower
Latency

↗ Improved Memory Organization
for Better Resource Sharing

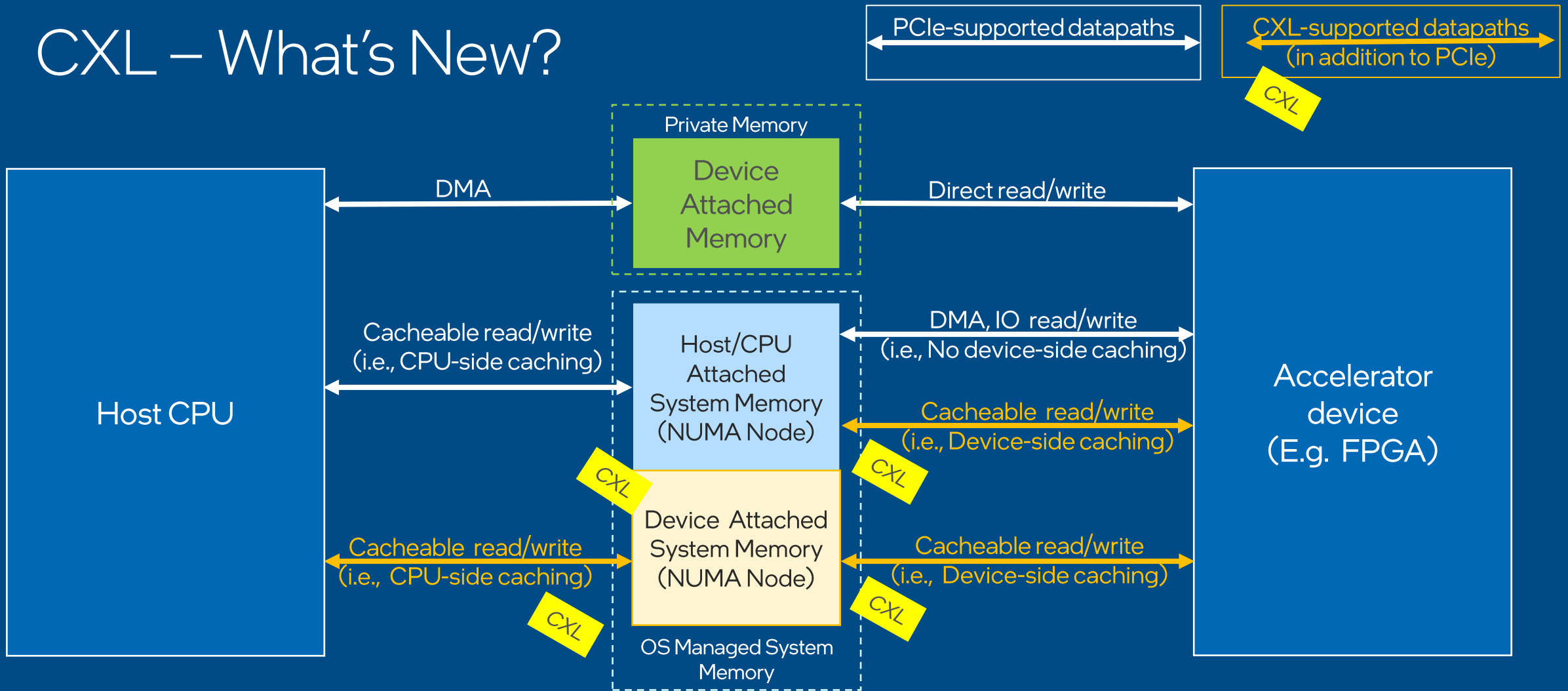
Compute Express Link (CXL) – Overview & Latest News



- What is CXL? **An open-source coherent interconnect protocol** (re-uses PCIe PHY/data layers)
- Who is in CXL.org? **Over 200 members & growing**
- Latest News:
 - Gen-Z Consortium joined CXL & transferred assets/technology
 - OpenCAPI Consortium letter of intent to join CXL
 - CXL joins open fabric management frameworks (DMTF, OFA, SNIA)

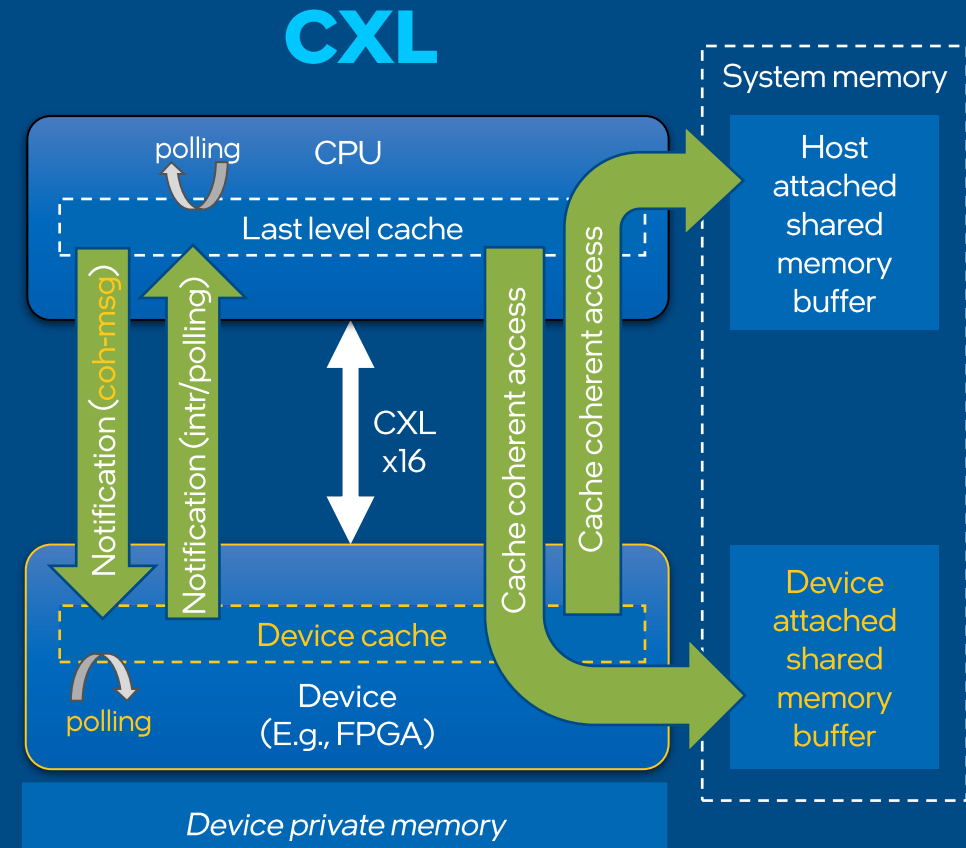
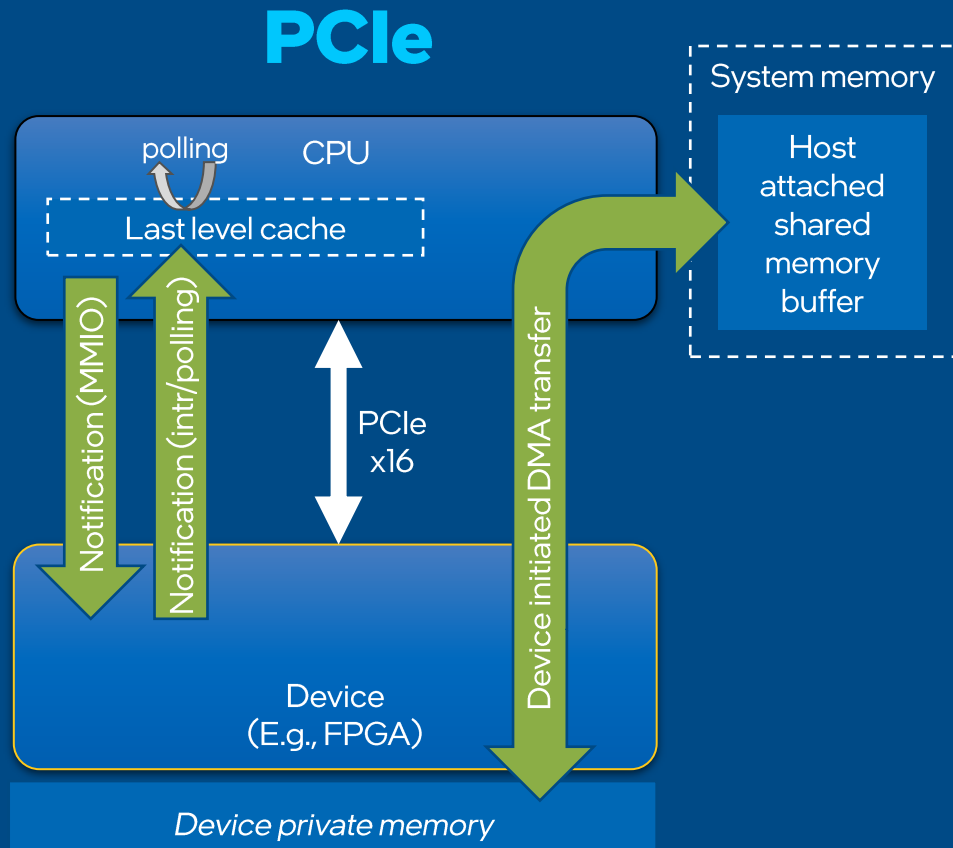
<https://www.computeexpresslink.org/>

CXL – What's New?



CXL-based accelerators elevated to 1st class priority

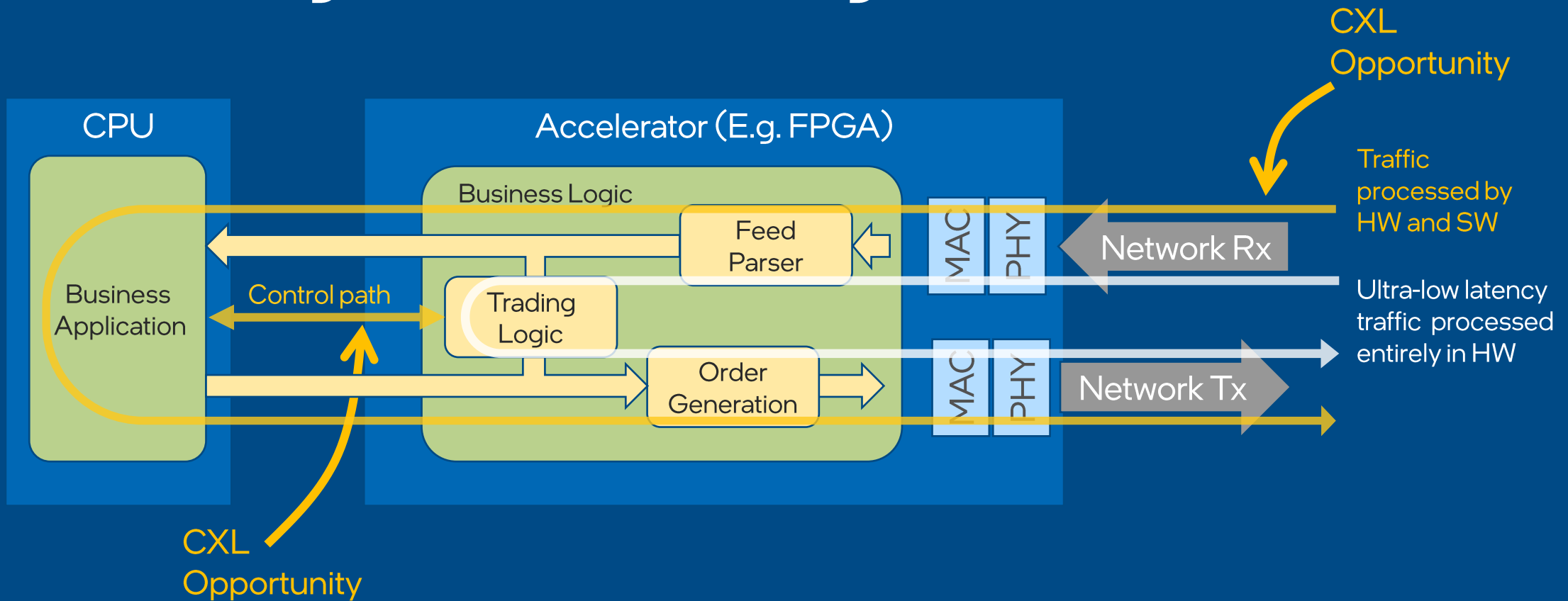
CXL Accelerators – Common Shared Cache/Memory



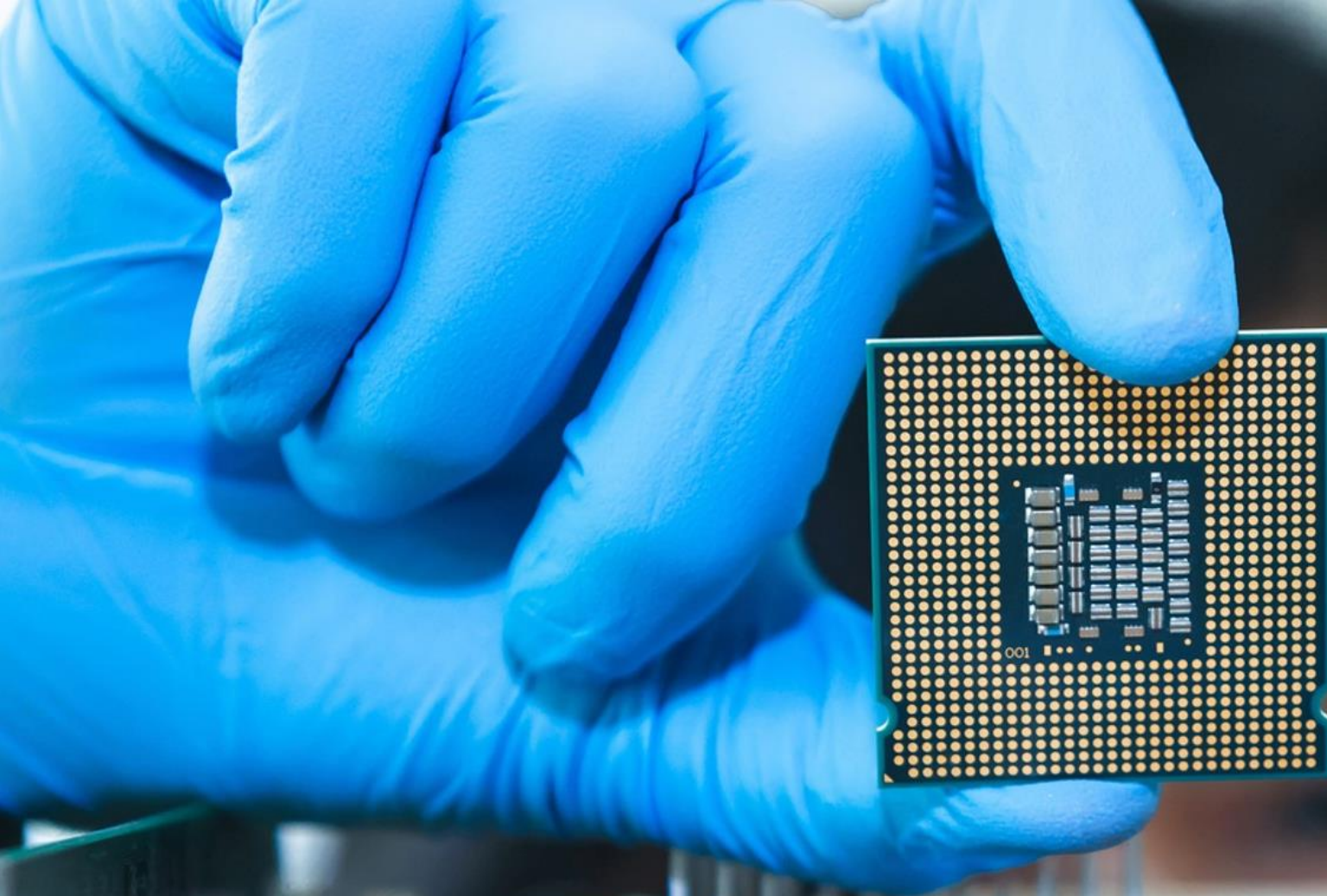
CXL enables:

- Low latency notifications using coherency semantics (*new*)
- Device-side polling (*new*)
- Shared memory buffers cache coherently accessible by CPU and device (*new*)

Accelerating Securities Trading



CXL enables tightly coupled CPU-HW interactions, resulting in better use of CPU and hence helping reduce accelerator complexity



Intel® Agilex™ FPGA

- 1st & only FPGA with CXL hard IP
- 4x higher CXL bandwidth per port vs. other FPGA CXL implementations¹
- CXL 1.1 and 2.0 (see schedule)

¹ Learn more at www.intel.com/PerformanceIndex (see the FPGA section for workloads and configurations). Results may vary.

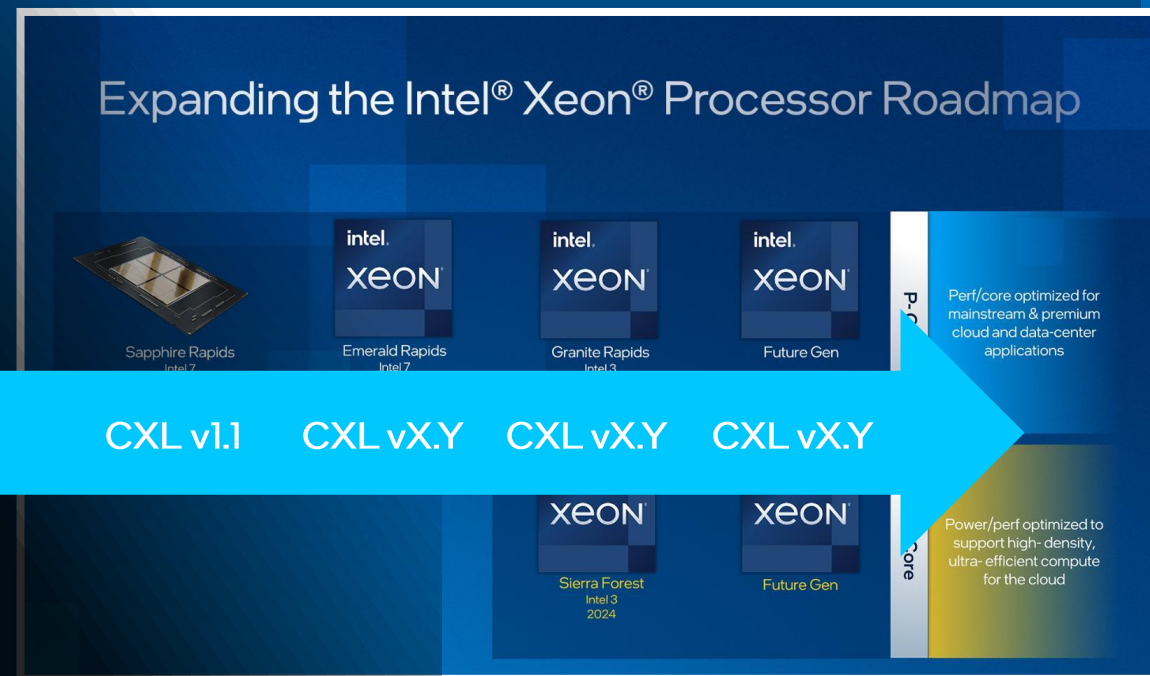
CXL-Capable HW & Ecosystem

Contact OEM/ODM

- ✓ Server embargo release dates under CNDA
- ✓ Based on 4th Gen Intel® Xeon® Scalable processor (formerly codenamed Sapphire Rapids)

Start CXL R&D now!

- ✓ Choose your production intercept
- ✓ Intel FPGA offers SW upgrade CXL 1.1 to 2.0
- ✓ Choose from a variety of Intel FPGA devices & board options

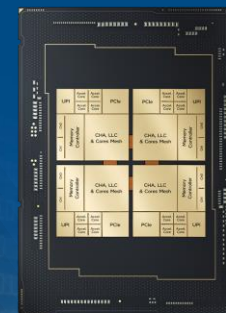


Source: Intel Investor Day (Feb. 17, 2022)

Intel Agilex FPGAs – Leading Financial Services

Leadership with CXL

- ✓ 1st and only FPGA with CXL hard IP
- ✓ FPGA HW supports CXL 1.1 and 2.0



Strategic Collaboration with LMS

ÜberNIC™ Exclusively Based on Intel Agilex FPGAs

- ✓ Fully hardware network stack with CXL
- ✓ Truly supports modern market data rates



Attend LMS session today

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- ¹ Intel estimates based on Agilix FPGA CXL hard + soft IP test results (CXL link at Gen 5 x16) vs. Xilinx FPGA using 3rd party CXL soft IP (CXL link at Gen4x8), both interop with pre-production 4th Gen Intel Xeon processors.

The Intel logo is centered on a solid blue background. It features the word "intel" in a white, lowercase, sans-serif font. A small, light blue square is positioned above the first vertical stroke of the letter 'i'. To the right of the word "intel" is a small white registered trademark symbol (®).

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