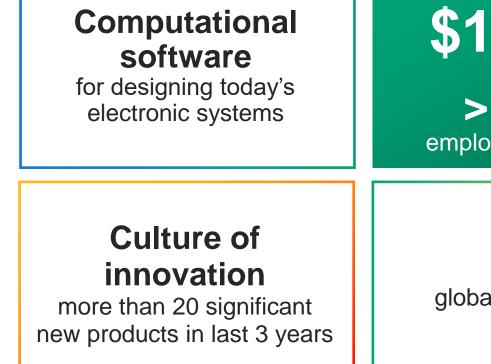
## Staying Cool at Speed: Adding 25G to HFT Accelerators

STAC Summit Chicago Ken Willis – Application Engineering Group Director May 30, 2024

### **Cadence Overview**

# Leading provider of Intelligent System Design<sup>™</sup> solutions Software, hardware, and IP that turn design concepts into reality



# Q1 2024 revenue: \$1.009B

>11,200 employees worldwide

# 26

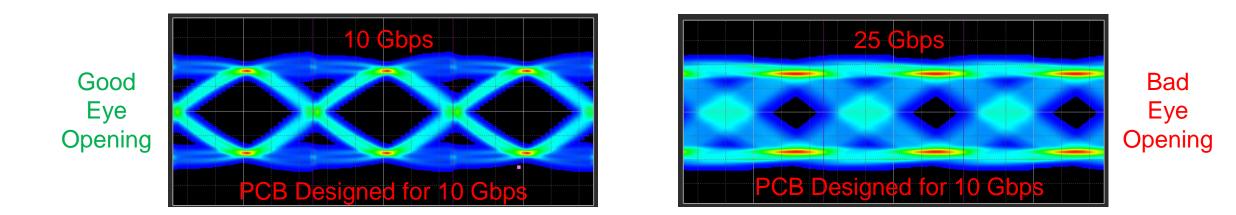
global development centers

cādence

Nasdaq: CDNS; S&P 500 and Nasdaq 100 indexes

Source: Cadence Earnings Press Release, April 22, 2024 https://www.cadence.com/en\_US/home/company/newsroom/press-releases/pr-ir/2024/cadence-reports-first-guarter-2024-financial-results.html

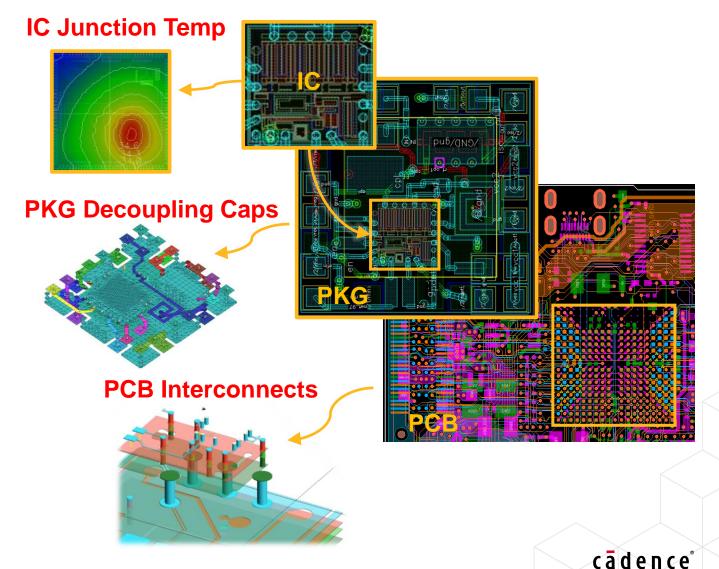
### How Does 25Gbps Differ from 10Gbps?



- Signal, Power, and Thermal Integrity become much more challenging at 25Gbps
- Fast rise times and higher data rates  $\Rightarrow$  interconnects become transmission lines
- Power Distribution Network (PDN) needs to support low voltage and high current
- Increased power dissipation leads to higher junction temperatures, thermal hot spots

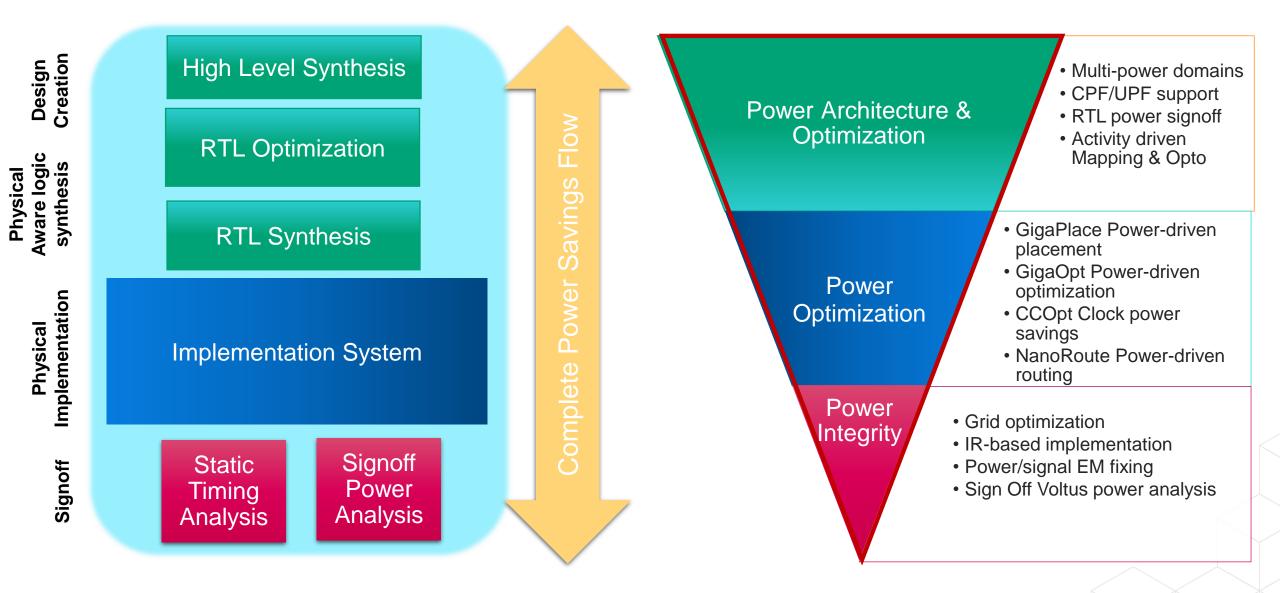
### Where can Power, Thermal, and SI Issues Exists in IC, Pkg, PCB?

- At high-speeds need to consider routing at all levels: IC, PKG, PCB
- Fast data rates means higher power, increased current densities and higher temperatures
- Minimize loop inductance with decoupling capacitors at the package
- Optimize signal routes, via structures, return paths, PDN on PCB



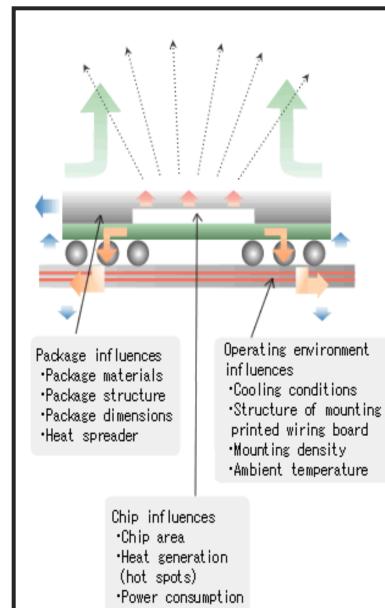
### IC Power Optimization Has to Be Full Flow

#### **Optimize Power**



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### Thermal Basics – 3 Modes of Heat Transfer



#### Radiation:

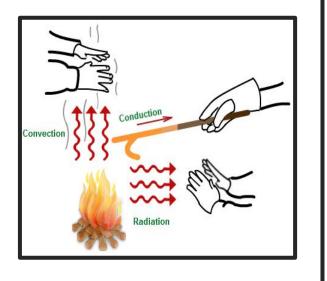
Heat transfer through the emission of the electromagnetic waves

#### Convection:

Heat transfer from a solid to a fluid, and a phenomenon in which heat moves throughthe fluid

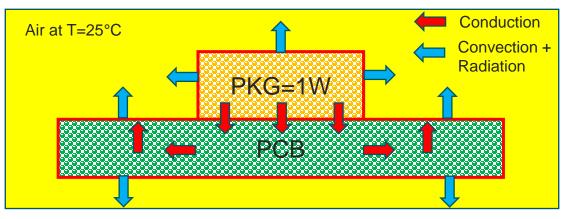
#### Conduction:

Heat transfer by which heat passes through a material The vibrations of the molecules in a lattice, or the transportation by free electrons

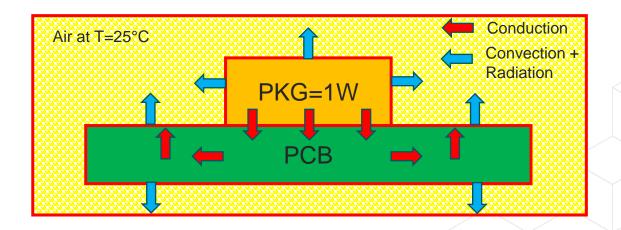


### Thermal Basics – FEA vs. CFD

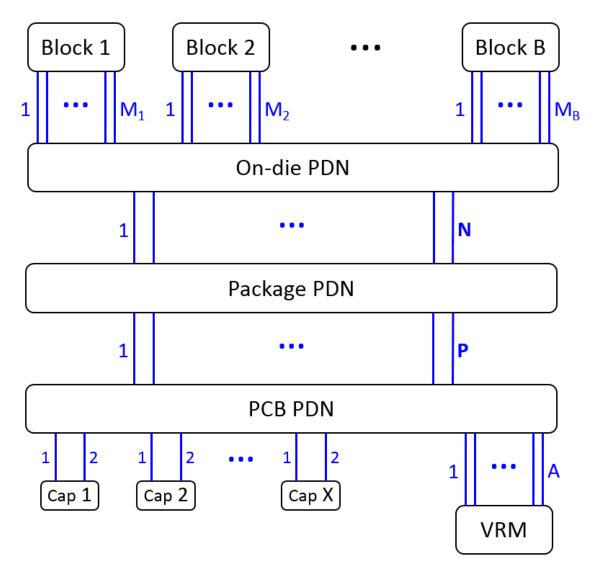
- FEA (Finite Element Analysis): in the context of thermal, it is used to solve conduction problems within solids in detail with convection and radiation effect taken into account in a simplified manner with a boundary condition of heat transfer coefficient.
  - FEA allows detailed and accurate conduction analysis
  - FEA simplifies convection and radiation with a boundary condition with a heat transfer coefficient (no actual simulation of a fluid)

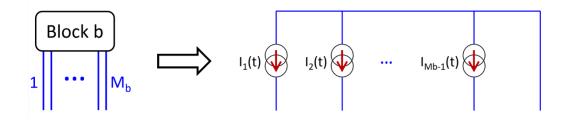


- **CFD (Computational Fluid Dynamics):** in the context of thermal, it is used to solve conduction in a simplified manner (typically) and convection and radiation in detail by actual simulation of fluid flow (e.g.) fan blowing air over a PCB)
  - CFD allows conduction analysis with simplified structures typically.
  - CFD does the actual detailed simulation of convection and radiation. There is no boundary condition of heat transfer coefficient



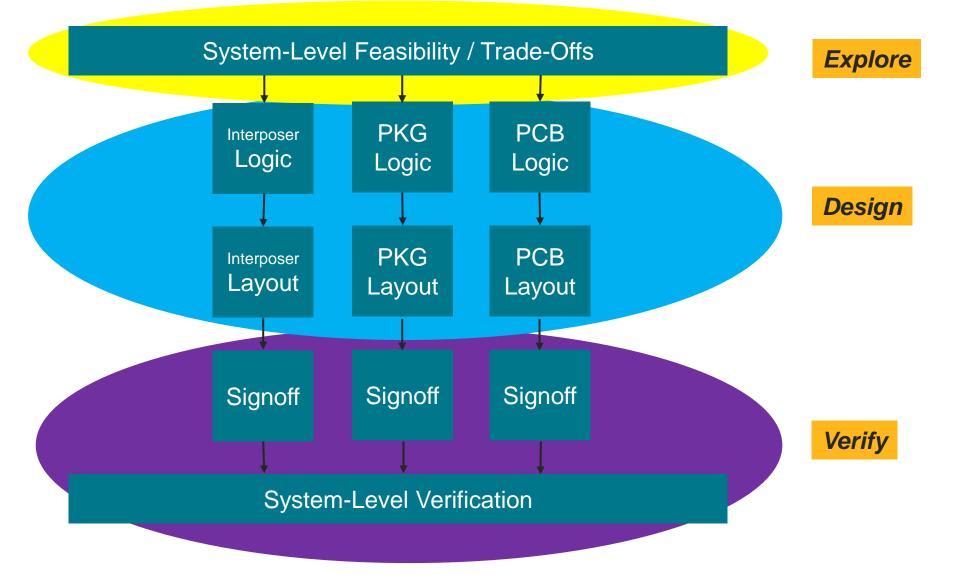
### What Power Distribution Network (PDN) Does Your Chip See?



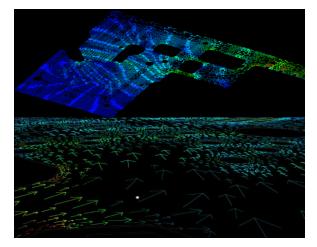


- "Clean" power comes into PCB
- Travels through multiple levels of parasitics
- Non-ideal power delivered to chip

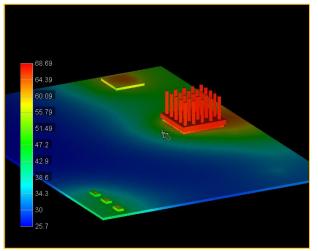
### How do you address this? Multiple levels to consider ...



### IR Drop Analysis of Package / PCB



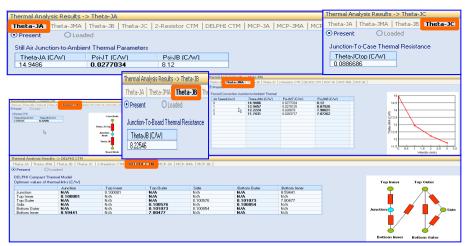
#### IR Drop Analysis



E/T Co-Simulation

Resistance Name	Model	🖶 📛 Positive Pin (GND)	-	Pin1 Name	Pin1 Net	Pin2 Name	Pin2 Net	Resistance (Oh
RESI BGA1 DIE1 VDDIO	Multiple to Multiple	196PINEGA_EGA1.A1 (GND)			rvet		Net	
RESI BGA1 DIE1 GND	Multiple to Multiple			Node0!!A1::GND	GND	Node2527!!SWSIG8	GND	0.002650
		C 196PINBGA_BGA1.A2 (GND) D 196PINBGA_BGA1.A3 (GND)		Node0!!A1::GND	GND	Node2596!!SESIG3	GND	0.002661
		196PINBGA_BGA1.A3 (GND) 196PINBGA_BGA1.A4 (GND)		Node0!!A1::GND	GND	Node2458!!NWSIG3	GND	0.00268
		I96PINBGA_BGA1.A4 (GND) I96PINBGA .BGA1.A5 (GND)	=	Node0!!A1::GND	GND	Node2389!!NESIG8	GND	0.00270
		E C 196PINBGA_BGA1.A6 (GND)		Node0!!A1::GND	GND	Node2525!!SWSIG8	GND	0.00274
		() (C) 196PINBGA _BGA1.AG (GND)		Node0!!A1::GND	GND	Node2521!!SWSIG7	GND	0.00275
		(0.0) (0.0) (0.0) (0.0) (0.0)		Node0!!A1::GND	GND	Node2594!!SESIG2	GND	0.00276
		. C 196PINBGA .BGA1.A9 (GND)		Node0!!A1::GND	GND	Node2590!!SESIG3	GND	0.00276
		196PINBGA .BGA1.A10 (GND)		Node0!!A1::GND	GND	Node2456!!NWSIG2	GND	0.00279
		B C 196PINBGA .BGA1.A11 (GND)		Node0!!A1::GND	GND	Node2452!!NWSIG3	GND	0.00280
				Node0!!A1::GND	GND	Node2383!!NESIG7	GND	0.00280
				Node0!!A1::GND	GND	Node2523!!SWSIG8	GND	0.00280
				Node0!!A1::GND	GND	Node2387!!NESIG8	GND	0.00281
		I96PINBGABGA1.B1 (GND)		Node0!!A1::GND	GND	Node2515!!SWSIG6	GND	0.00283
		B C 196PINBGA_BGA1.B2 (GND)		Node0!!A1::GND	GND	Node2584!!SESIG3	GND	0.0028
		I96PINBGA_BGA1.B3 (GND)		Node0!!A1::GND	GND	Node2592!!SESIG1	GND	0.00283
		I96PINBGA_BGA1.84 (GND)		Node0!!A1::GND	GND	Node2532!!SWSIG8	GND	0.00284
		IB-C 196PINBGABGA1.B9 (GND)		Node0!!A1::GND	GND	Node2579!!SESIG3	GND	0.00286
		① 196PINBGABGA1.B10 (GND)		Node0!!A1::GND	GND	Node2510!!SWSIG5	GND	0.00287
		① 196PINBGA_BGA1.B11 (GND)		Node0!!A1::GND	GND	Node2454!!NWSIG1	GND	0.00287
		196PINBGA_BGA1.B12 (GND) 196PINBGA_BGA1.B13 (GND)		Node0!!A1::GND	GND	Node2538!!SWSIG8	GND	0.00287
				Node0!!A1::GND	GND	Node2601!!SESIG8	GND	0.00288
		196PINBGA_BGA1.B14 (GND)		Node0!!A1::GND	GND	Node2377!!NESIG6	GND	0.0028
		(C) 196PINBGA_BGA1.C1 (GND)		Node0!!A1::GND	GND	Node2574!!SESIG3	GND	0.00288
		() (C) 196PINEGA_BGA1.C13 (GND)		Node0!!A1::GND	GND	Node2446UNWSIG3	010	0.002893

#### Resistance Measurement



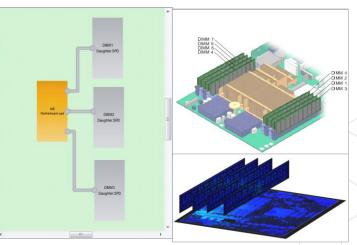
Thermal Model Extraction

#### Resistance Analysis Setup -> Set up Eq. Resistance Netw Add Terminal Delete Terminal Change Output File... 🗹 Use File Name Pattern 🔄 Short VRM 🔄 Other Circuit Output File Name: D:\Cadence\Sigrity2019\share\SpeedXP\Samples\PowerDC\Electrical Analysis\SpiceNetlist.ckt - C 200UM DIE DIEL NESIG1001 (VODIO). Terminal Name JIG4003 DIEJ SWSIG5003 DIE1 SWSIG5003 GND -1.400000000000000 SWSIG6003 DIE1 SWSIG6003 GND -1.4000000000000000 DIE1.NESIG1003 \*SWSIG5003 DIE1\_SWSIG7003 GND -1.4000000000000 \*SWSIG8001 DIE1\_SWSIG8001 GND -1.00000000000000 DIE1.NESIG2001 \*SWSIG8002 DIE1 SWSIG8002 GND -1.20000000000000 -1.400 DIE1.NESIG2003 \*SWSIG8003 DIE1\_SWSIG8003 GND -1.40000000000000 -1.4000 \*SWSIG8004 DIE1\_SWSIG8004 GND -0.80000000000000 -1.40000 \*SWSIG8005 DIE1\_SWSIG8005 GND -0.60000000000000 -1.40000 DIE1 NESIG3001 DIE1.NESIG3003 \*SWSIG8006 DIE1 SWSIG8006 GND -0.40000000000000 -1.4000 SWSIG8007 DIE1\_SWSIG8007 GND -0.20000000000000 -1.400 DIE1.NESIG4001 DIE1.NESIG4003 DIE1.NESIG5001 \* [MCP End] DIE1.NESIG5003 \*This concludes the MCP section DIE1.NESIG600 PO DTEL NESTG2001 DTEL NESTG1001 0.020925908437 DIE1.NESIG6003 RO DEL MESIG2001 DEL MESIG2001 0.02/02/09/0543/5 RI DEL MESIG3001 DEL MESIG2001 0.02/008917714 R2 DEL MESIG5001 DEL MESIG2001 0.0364826726036 R3 DEL MESIG5001 DEL MESIG2001 0.0658278338151 DIE1 NESIG6004 DIE1.NESIG600 R4 DIEL MESIGG001 DIEL MESIG2001 0.145774201352 R5 DIEL MESIG6004 DIEL MESIG2001 0.139203469084 R6 DIEL MESIG6005 DIEL MESIG2001 0.230447970495 DIE1.NESIG6006 DIE1.NESIG6007 R7 DIE1 NESIG6006 DIE1 NESIG2001 0.356908964673 R7 DEL MESIGGOO DEL MESIGGOOI 0.35660864673 R8 DIEL MESIGGOOT DEL MESIGGOOI 0.252894148984 R9 DIEL MESIGGOOT DEL MESIGGOOI 0.766041404246 R10 DEE MESIGGOOI DEL MESIGGOOI 1.0584204857 R11 DEL MESIGGOOI DEL MESIGGOOI 1.55148668244 R21 DEL MESIGGOOI DEL MESIGGOOI 3.25093536934 DIE1.NESIG7003 DIE1 NESIG8001 DIE1.NESIG8002 DIE1.NESIG8003 DIE1.NESIG8004 R14 DIEL NWSIG1006 DIEL NESIG2001 6.88715063143 R15 DIEL\_WRSIG400 DIEL\_WESIG2001 6.02463145945 R15 DIEL\_WRSIG4001 DIEL\_WESIG2001 6.02463145945 R16 DIEL\_WRSIG6001 DIEL\_WESIG2001 13.103080432 R15 DIEL\_WRSIG6001 DIEL\_WESIG2001 17.1267667220 DIE1.NESIG8005 DIE1.NESIG8006

DIE1.NESIG8007

#### Resistance Network Generation

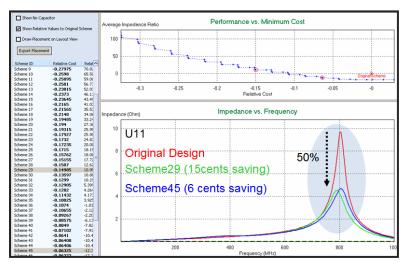
R19 DIE1 SESIF1004 DIE1 NESIG2001 0.48181232888



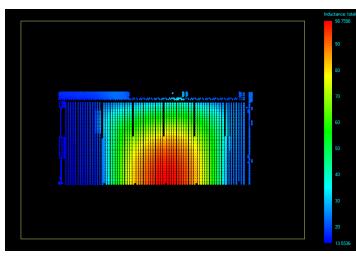
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Multi-Board Analysis

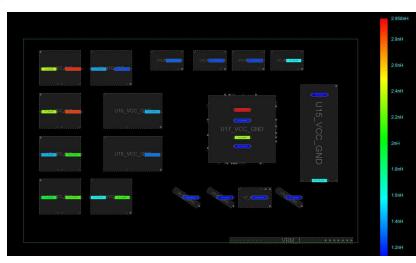
### AC Analysis of Package / PCB



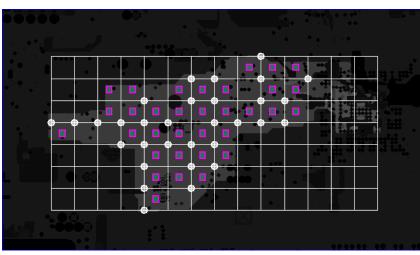
Pre- and Post-Layout Optimization



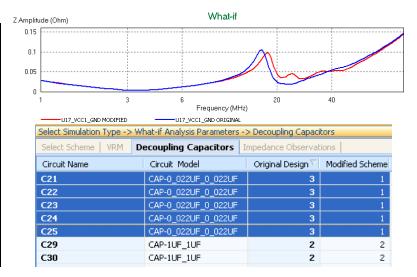
IC Device Power Pin Inductance



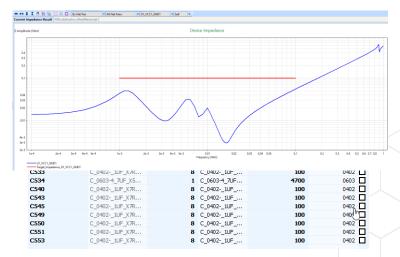
### Decoupling Capacitor Loop Inductance



EMI Capacitor Optimization



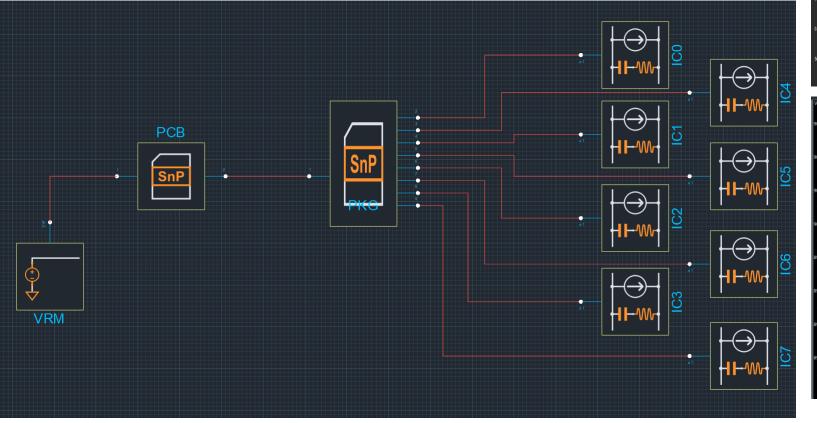
#### What-if Analysis

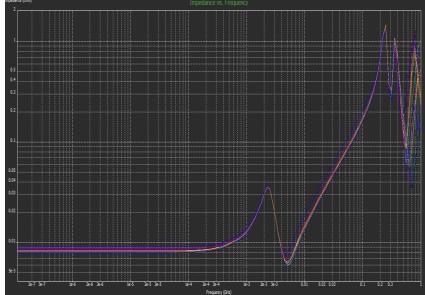


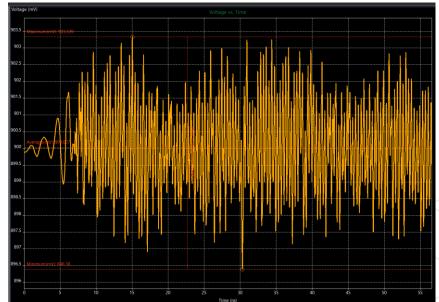
### PDN Impedance Check

### System-Level PI Analysis

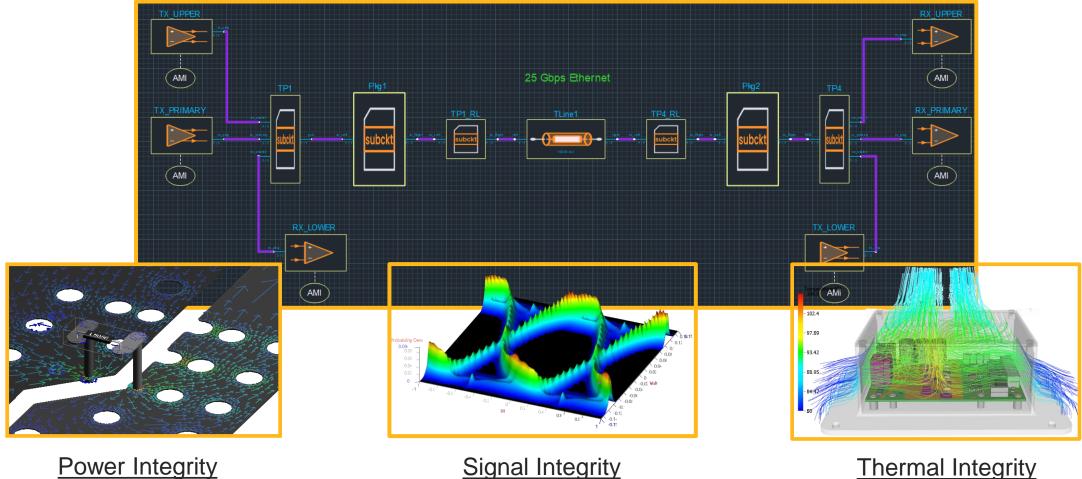
- Put packages and PCB(s) all together for complete PDN
- Check frequency domain vs. target impedance
- Check time domain vs. ripple spec







### Cadence MSA Technology Enables High-Speed Operation



Operate at low supply voltages Eliminate high current density spots Meet PDN AC impedance

### Signal Integrity

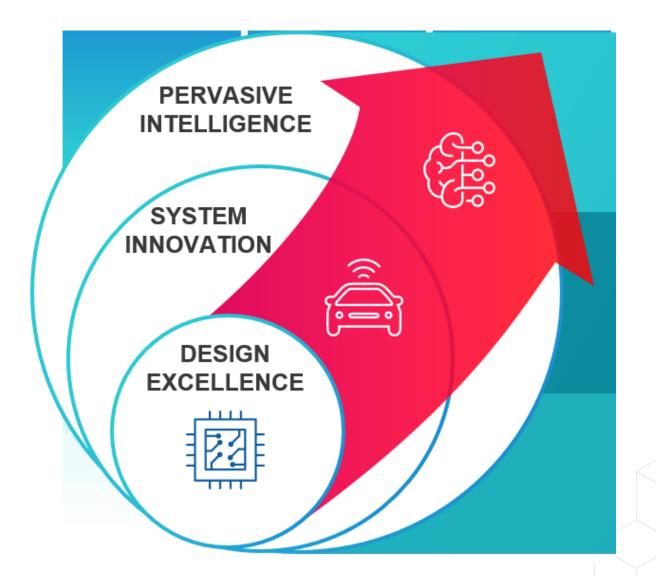
Optimized Signal/Return-path routing Minimize reflections and crosstalk Validate System Compliance

**Thermal Integrity** 

Guarantee Junction Temperatures Eliminate thermal hot spots Optimize system cooling cādence

### **Staying Cool Summary**

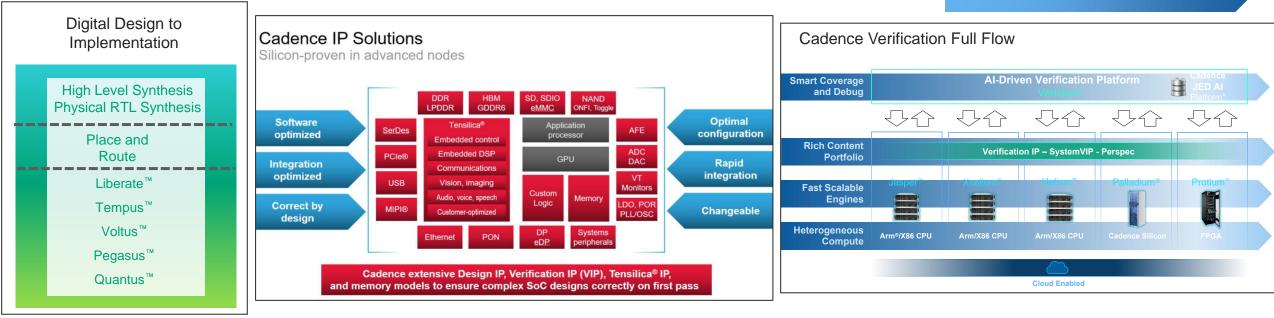
- Signal, Power, and Thermal Integrity become much more challenging at high-speeds
- Fast data rates means higher power consumption, increased current densities, and higher temperatures must be considered in the design process
- High-speed signal routes, via structures, return paths must be designed with transmission lines and modeled with electromagnetic extractions
- The complexity of high-performance systems design is an iterative, resource intensive, and expensive process that can benefit from AI driven analysis
- Cadence offers the complete solution of design platforms, multi-physics analysis engines, and is now bringing AI to bear on the system design problem



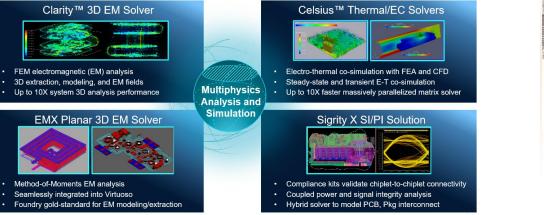
### **Cadence: HFT Accelerator Partner**

## Contact us: hft@cadence.com

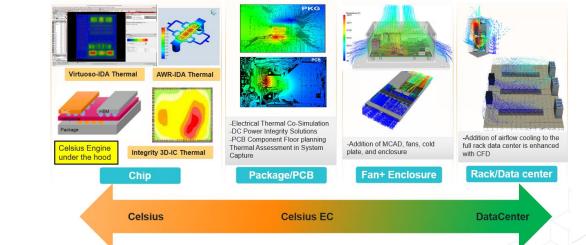
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#### Cadence Multiphysics Simulation and Analysis Technology



#### Thermal Analysis Solutions from Chip to Systems



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