

Do you *really* know what happens inside your FPGA?



# What we do...

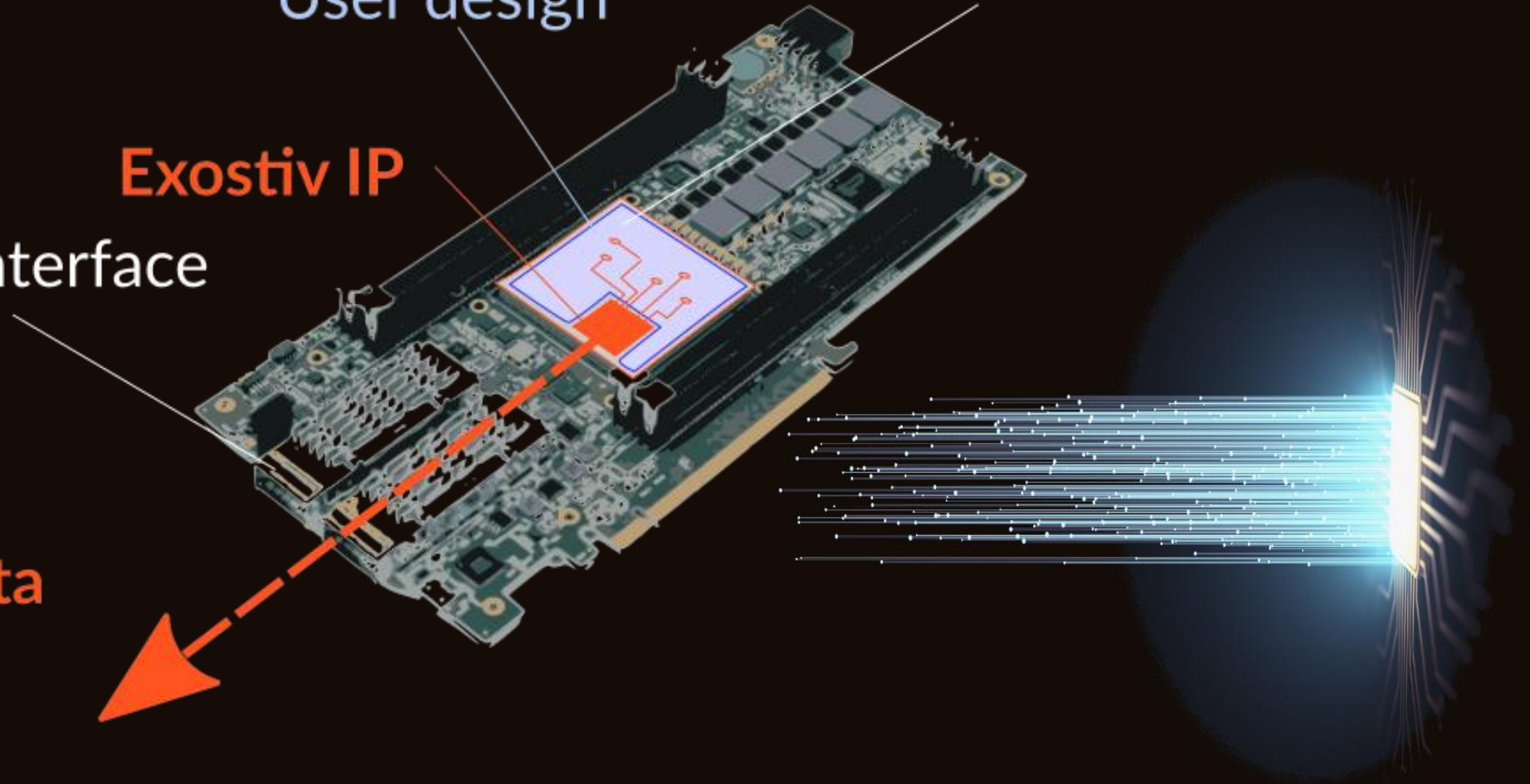
Target FPGA

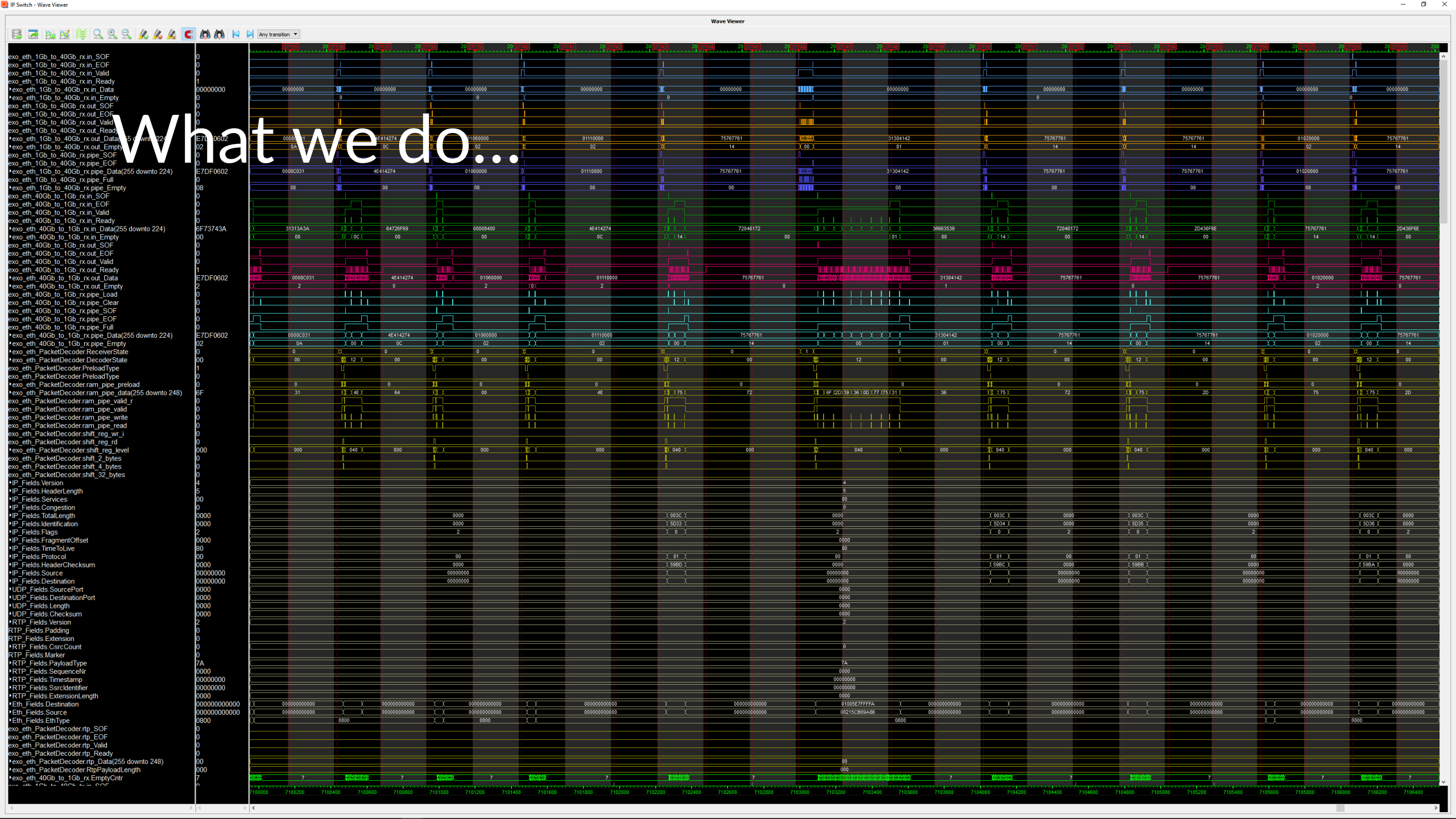
User design

Exostiv IP

High speed interface

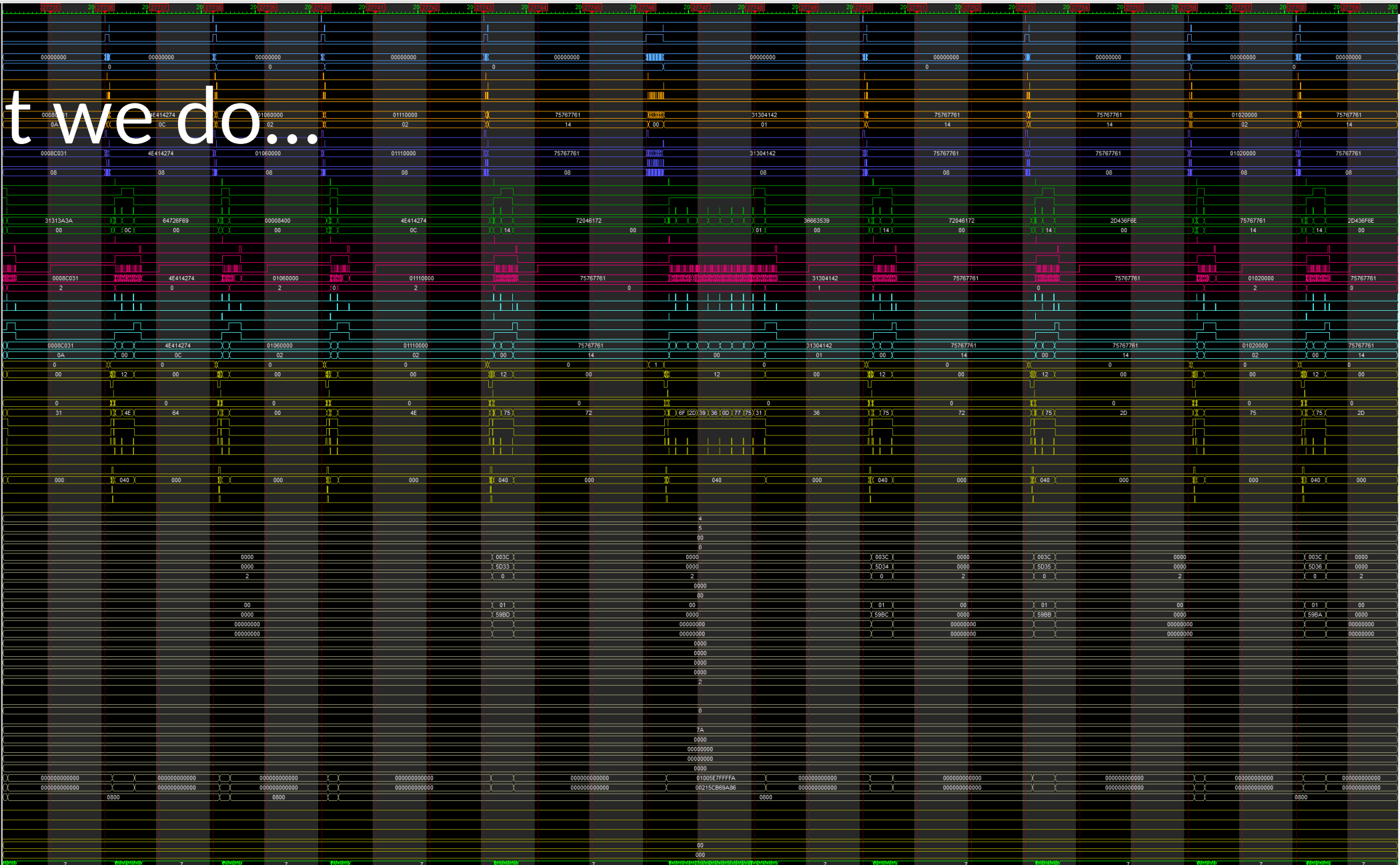
Trace data  
Alerts  
Events





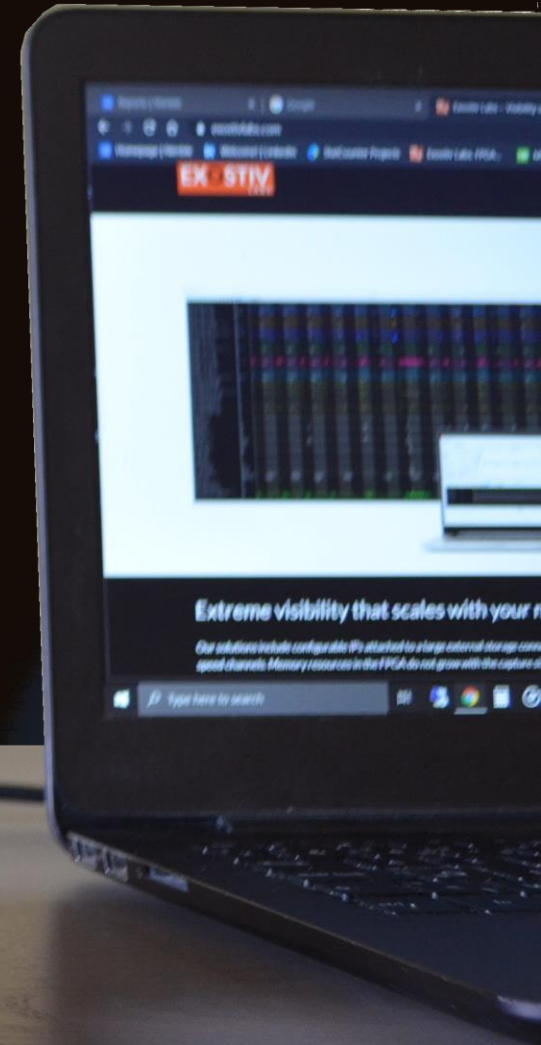
What we do...

```
exo_eth_1Gb_to_40Gb_rx.in_SOF 0
exo_eth_1Gb_to_40Gb_rx.in_EOF 0
exo_eth_1Gb_to_40Gb_rx.in_Valid 0
exo_eth_1Gb_to_40Gb_rx.in_Ready 1
*exo_eth_1Gb_to_40Gb_rx.in_Data 00000000
*exo_eth_1Gb_to_40Gb_rx.in_Empty 0
exo_eth_1Gb_to_40Gb_rx.out_SOF 0
exo_eth_1Gb_to_40Gb_rx.out_EOF 0
exo_eth_1Gb_to_40Gb_rx.out_Valid 0
exo_eth_1Gb_to_40Gb_rx.out_Ready 0
*exo_eth_1Gb_to_40Gb_rx.out_Data(5 down to 22) E7D0602
*exo_eth_1Gb_to_40Gb_rx.out_Empty 02
exo_eth_1Gb_to_40Gb_rx.pipe_SOF 0
exo_eth_1Gb_to_40Gb_rx.pipe_EOF 0
*exo_eth_1Gb_to_40Gb_rx.pipe_Data(255 downto 224) E7D0802
*exo_eth_1Gb_to_40Gb_rx.pipe_Full 08
*exo_eth_1Gb_to_40Gb_rx.pipe_Empty 08
exo_eth_40Gb_to_1Gb_rx.in_SOF 0
exo_eth_40Gb_to_1Gb_rx.in_EOF 0
exo_eth_40Gb_to_1Gb_rx.in_Valid 0
exo_eth_40Gb_to_1Gb_rx.in_Ready 0
*exo_eth_40Gb_to_1Gb_rx.in_Data(255 downto 224) 8F73743A
*exo_eth_40Gb_to_1Gb_rx.in_Empty 00
exo_eth_40Gb_to_1Gb_rx.out_SOF 0
exo_eth_40Gb_to_1Gb_rx.out_EOF 0
exo_eth_40Gb_to_1Gb_rx.out_Valid 0
exo_eth_40Gb_to_1Gb_rx.out_Ready 1
*exo_eth_40Gb_to_1Gb_rx.out_Data E7D0602
*exo_eth_40Gb_to_1Gb_rx.out_Empty 0
exo_eth_40Gb_to_1Gb_rx.pipe_Load 0
exo_eth_40Gb_to_1Gb_rx.pipe_Clear 0
exo_eth_40Gb_to_1Gb_rx.pipe_SOF 0
exo_eth_40Gb_to_1Gb_rx.pipe_EOF 0
exo_eth_40Gb_to_1Gb_rx.pipe_Full E7D0602
*exo_eth_40Gb_to_1Gb_rx.pipe_Data(255 downto 224) 02
*exo_eth_PacketDecoder_ReceiverState 0
*exo_eth_PacketDecoder_DecoderState 00
exo_eth_PacketDecoder_PreloadType 1
exo_eth_PacketDecoder_PreloadType 0
*exo_eth_PacketDecoder_ram_pipe_preload 8F
*exo_eth_PacketDecoder_ram_pipe_data(255 downto 248) 31
*exo_eth_PacketDecoder_ram_pipe_valid_r 0
exo_eth_PacketDecoder_ram_pipe_valid 0
exo_eth_PacketDecoder_ram_pipe_write 0
exo_eth_PacketDecoder_ram_pipe_read 0
exo_eth_PacketDecoder_shift_reg_wr_j 0
exo_eth_PacketDecoder_shift_reg_rd 0
*exo_eth_PacketDecoder_shift_reg_level 000
exo_eth_PacketDecoder_shift_2_bytes 0
exo_eth_PacketDecoder_shift_4_bytes 0
exo_eth_PacketDecoder_shift_32_bytes 5
*IP_Fields_Version 4
*IP_Fields_HeaderLength 5
*IP_Fields_Services 00
*IP_Fields_Congestion 0
*IP_Fields_TotalLength 0000
*IP_Fields_Identifier 0000
*IP_Fields_Flags 2
*IP_Fields_FragmentOffset 0000
*IP_Fields_TimeToLive 80
*IP_Fields_Protocol 00
*IP_Fields_HeaderChecksum 0000
*IP_Fields_Source 00000000
*IP_Fields_Destination 00000000
*UDP_Fields_SourcePort 0000
*UDP_Fields_DestinationPort 0000
*UDP_Fields_Length 0000
*UDP_Fields_Checksum 0000
*RTP_Fields_Version 2
RTP_Fields_Padding 0
RTP_Fields_Extension 0
RTP_Fields_CsrCount 0
RTP_Fields_Marker 0
*RTP_Fields_PayloadType 7A
*RTP_Fields_SequenceNr 0000
*RTP_Fields_Timestamp 00000000
*RTP_Fields_SsrcIdentifier 00000000
*RTP_Fields_ExtensionLength 0000
*Eth_Fields_Destination 000000000000
*Eth_Fields_Source 000000000000
exo_eth_PacketDecoder_rtp_SOF 0
exo_eth_PacketDecoder_rtp_EOF 0
exo_eth_PacketDecoder_rtp_Valid 0
exo_eth_PacketDecoder_rtp_Ready 0
*exo_eth_PacketDecoder_rtp_Data(255 downto 248) 00
*exo_eth_PacketDecoder_rtpPayloadLength 000
*exo_eth_40Gb_to_1Gb_rx.EmptyCnt 7
```

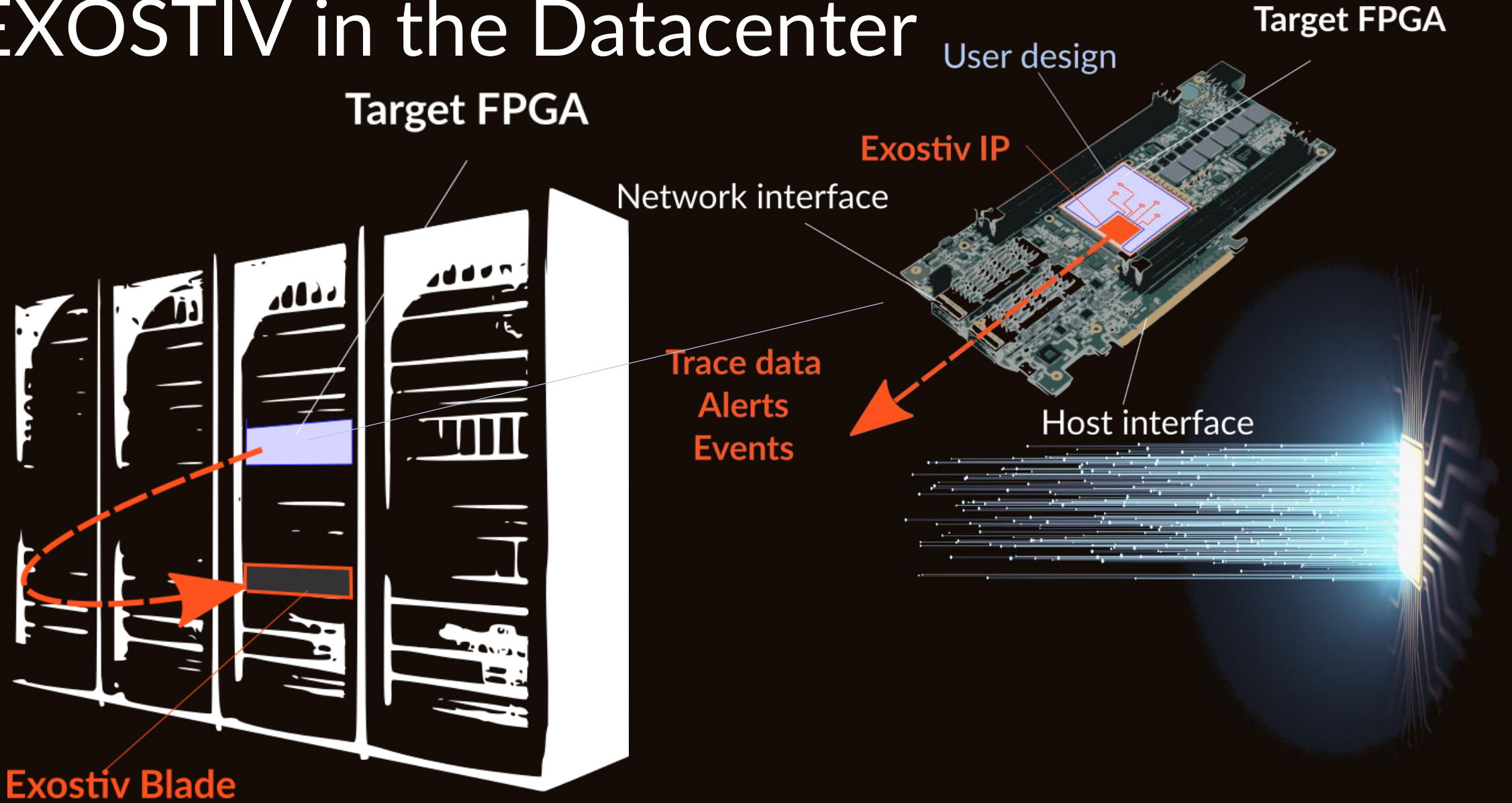


# EXOSTIV in the lab

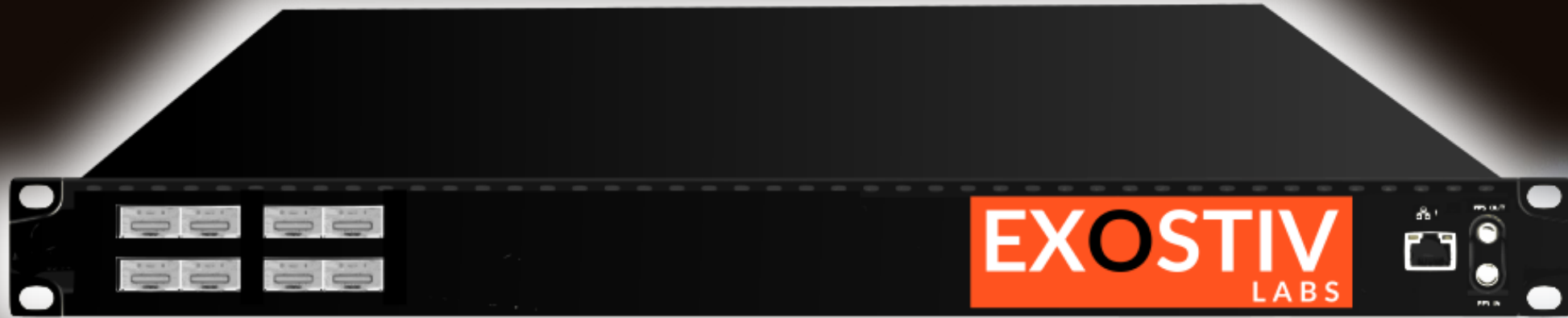
- 32K nodes per FPGA max
- 8 GB memory
- 50 Gbps bandwidth
- > 350 MHz operation
- Data multiplexing, triggering, filtering, event counters
- Integrated waveform viewer
- Xilinx Series 7, Ultrascale(+), Zynq / Intel Series 10 support



# EXOSTIV in the Datacenter




# EXOSTIV Blade

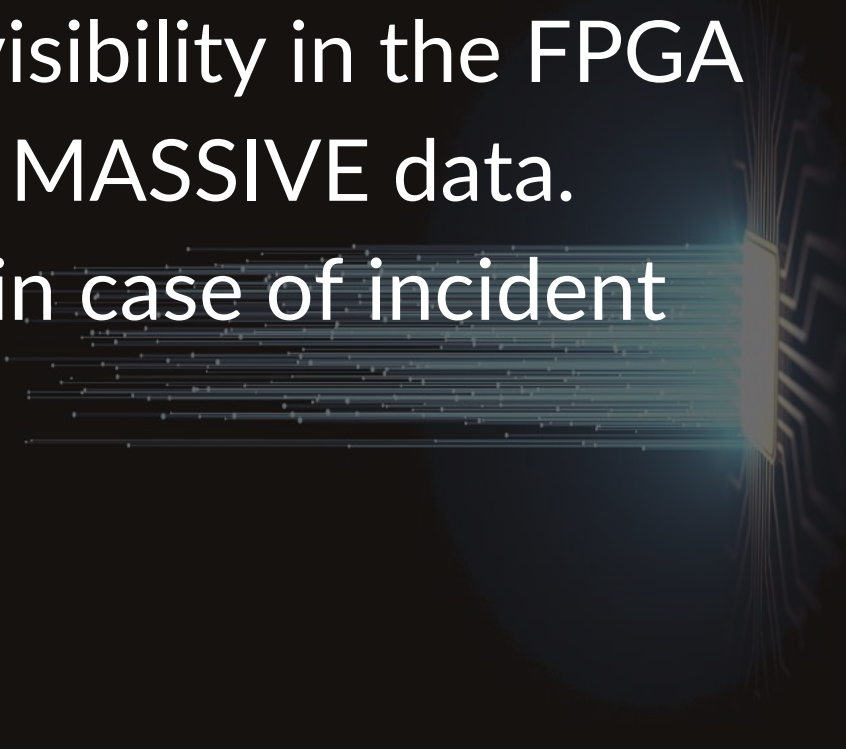


- Scale up to 1 Tbps - 80 GB memory - 10 x 100 Gbps QSFP+
- SSD local storage option or bridge to network storage

# Capabilities

- Alert generation & Trace capture from inside the FPGA
    - ✓ Cycle-accurate
    - ✓ User-defined
    - ✓ Data enrichment (timestamping, ...)
    - ✓ **Inside FPGA – NOT at I/O level**
  - Based on finance-grade hardware
  - **TERABYTES** of information with local storage.
  - Scales with technology: FPGA is its own observer
- 

# Benefits

- Fine-grain FPGA algorithms control & measurements
  - Visibility infrastructure available in the field & in the lab
  - Extremely detailed AND extended visibility in the FPGA
  - Algos assessment against REAL and MASSIVE data.
  - Faster corrections turnaround time in case of incident
- 



Thanks. Check the box for more info.

