# AMD

# High-Performance Trading with FPGA Accelerators, Low Latency NICs, and Server-Class Processors

Vasudevan Visvanathan Product Marketing

# STAC-T0 benchmark preliminary results<sup>1</sup> (AMD + Exegy)

### Why implement the benchmark?

- AMD performance claims quantified and validated
  - Specified application
  - Specified measurement method
  - Independent verification



1: Performance analysis performed by Exegy and audited by STAC Research. Results are preliminary and released with permission by STAC Research. Claims have not been independently verified by AMD. (Performance and latency are impacted by a variety of variables. Results are specific to Exegy IP and may not be typical. GD-181)

# **GTF versus GTY in T2T application (NOT STAC BENCHMARK)**

Hypothetical analysis to illustrate latencies in T2T system (Major latency contributors only)

## Not STAC Benchmark





■ Control word ■ Transceiver ■ MAC ■ Algorithm

#### How much lower T2T latency can be achieved?

Note: Hypothetical comparison based on common assumptions of latency of standard functions. Claims have not been independently verified by AMD. (Performance and latency are impacted by a variety of variables. GD-181)

# Introducing the Alveo<sup>™</sup> V80 for Big Data Compute

- First Broad-Market Versal<sup>™</sup> Accelerator Card Data analytics, Fintech, HPC, compute, storage, networking
- 2X Performance vs. Previous Gen<sup>1</sup>
  2X Memory Bandwidth, 2X Logic Density
- "Vivado<sup>™</sup> First" Design Flow
  New example design ("AVED") for ease of bring-up

## Launched May 8, 2024

1: Based on AMD published specifications for the Alveo U55C and Alveo V80 accelerator cards, as of March 2024. ALV-13

# AMD Solarflare<sup>™</sup> Low-latency Ethernet Adapters SOLARFLARE

Field-proven for Fintech networking



## 2x 10/25GbE

4x 10/25GbE

Proven Technology & Robust Roadmap

Deployed worldwide for 15+ years to 2500+ customers

Continuous improvements

Worldwide Support for Critical Applications

24/7 Support to meet compliance requirements

Long Term Support available

Custom Designed Performance Adapters

Targeted silicon design

Low-latency and high- performance hardware

Open Source, Robust Software Stack

Open Onload BSD API-compliant kernel bypass

TCPDirect optimized BSD API kernel bypass

ef\_vi link layer kernel bypass

# 4<sup>th</sup> Gen AMD EPYC CPUs for FinTech

#### **Trading Simulation & Research**

#### • Unprecedented core density To maximize throughput for embarrassingly parallel workloads (e.g., Monte Carlo methods)

#### • Large L3 caches

To improve performance for cache-bound applications (e.g., multifactor PDEs)

#### Updated IOD & AMD Gen3 Infinity Fabric<sup>™</sup>

To reduce latency for thread-distributed calculations & to enable higher CPU $\Leftrightarrow$ GPU bandwidth for heterogeneous applications (e.g., deep learning)







#### Machine Learning & Deep Learning

- New instruction set extensions BFLOAT16, VNNI, AVX-512 for improved AI capability
- Open-source software ecosystem
  Optimized AMD libraries for classical machine
  learning & inference

#### **Cloud Availability**

- 4<sup>th</sup> Gen AMD EPYC deployed across major CSPs
- Well-suited for burst workloads (e.g., regulatory scenarios)



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# **Disclaimer & Attribution**

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