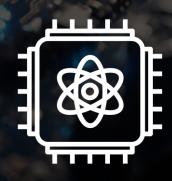


# TELESOFT – London STAC Summit, May 2024

Maximising Efficiency: Trade Cycle Optimisation









### **ABOUT TELESOFT**



HIGH RATE, ULTRA-LOW LATENCY PLATFORM

**UK DESIGN & MANUFACTURE** 



**ULTRA-LOW LATENCY** 



35+ YEARS OF **EXPERIENCE** 





**MARKET LEADING FPGA PROCESSING** 



HIGH RATE, **400GbE CAPABILITY** 



**GLOBAL DEPLOYMENTS** 













**TELESOFT** 









### HARDWARE CAPABILITIES





## Altera Agilex FPGA Accelerator

Delivering deterministic performance by accelerating multi-market data processing



# Precision Time Protocol (PTP)

Ensuring accurate time synchronisation to nanosecond resolution



### AI + ML Data Processing

Increasing processing efficiency by integrating established AI & ML models to spare FPGA resource



## **ARM Cortex-A53 Real-Time Processor**

Ensuring unparalleled execution on trade orders, risk management, and compliance checks



# Quantum Random Number Generator (QRNG) Chip

Utilising QRNG to enhance network security and encryption key generation



### **Inter-Card Connectivity**

PCIe gen5 x16 & CXL. All Ethernet standards up to 400GbE

### APPLICATIONS

# ALGORITHMIC TRADING

 Gain trading advantage by ingesting real-time market data into integrated AI & ML models



# MARKET DATA PROCESSING

Multi-Market, Single Device;
 Latency Not Impacted





### REAL-TIME RISK ANALYSIS

 Calculate RISK on Single Appliance



- Passive or Inline
- Nanosecond Visibility
- 1ms Microburst Analytics
- Gap Detection
- Latency Measurement
- Packet Capture





### CYBER SECURITY

- HRoT (Hardware Root
  - of Trust)
- Quantum Key
  - Generation
- Secure
  - Communication

### SOLUTION



SINGLE APPLIANCE WITH THE UNIQUE ABILITY TO PROGRAM EACH CARD WITH THE CAPABILITY YOU WANT, WHEN YOU WANT



Inter-Card Connectivity - Ethernet / PCIe / CXL

32 x 100GbE or 8 x 400GbE



CONSOLIDATE INFRASTRUCTURE

**REDUCE OPEX** 

MAXIMISE EFFICIENCY

### **USE CASES**



#### **NETWORKS**



- Route Optimisation
- Network Efficiency
- Consolidation
- Transparency
- Security

### INFRASTRUCTURE



- Identify & VisualiseBottlenecks inReal-Time
- Optimise, Load
   Balance

### MARKET DATA



- Trade Optimisation
- Never Miss a Packet
- Multi-Market SingleCard
- Real-Time Analytics
- Distribution
- Reporting

#### **TRADING**



- Trade CycleOptimisation
- Your Code, Your Chip
- Integration to AI & ML on a SingleAppliance

### **CYBER SECURITY**



- Hardware Root of
  - Trust (HRoT)
- Onboard QRNG
- Real-Time

Surveillance

### **SUMMARY**





**400GbE** Processing at Full Line Rate - Zero Packet Drops



Trading **IPs** including OPRA Engine @400Gbps





Advanced FPGA PCIe Boards Designed & Manufactured **In House** 



Products Designed
Specifically with Nanosecond
Accuracy, Ultra-High Throughput
and Ultra-Low Latency

Quantum Resistant **Cryptography** for
Securing Data Transfer



AI / ML FPGA Inferencing Engine



Engineering Led Company,
Offering **Customer Focused**,
Tailored Solutions &
Intergrations



