Staying Cool at Speed: Adding 25G to HFT Accelerators

STAC Summit London

Michael O’Sullivan – Engineering Director

May 2, 2024

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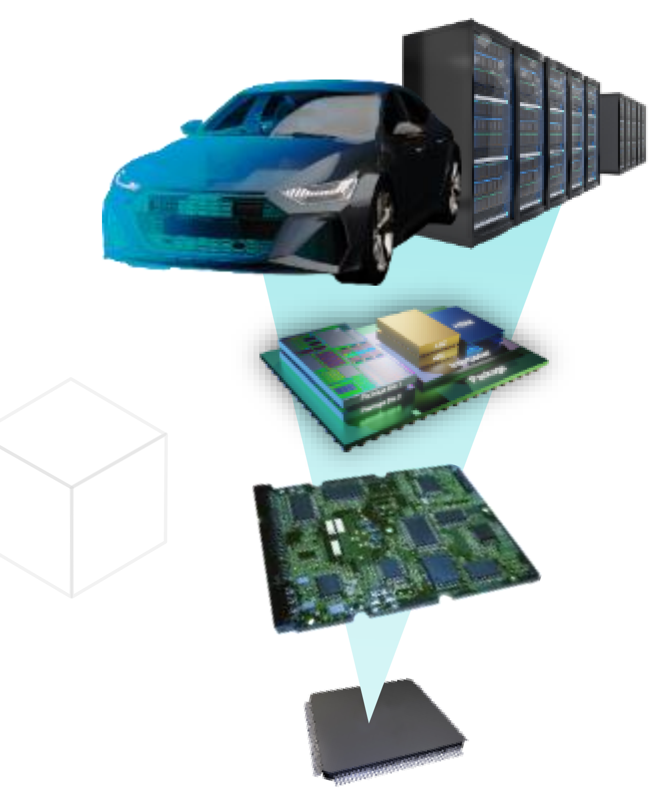
Cadence Overview

Leading provider of **Intelligent System Design™ solutions**
Software, hardware, and IP that turn design concepts into reality



Computational software
for designing today's electronic systems

Q1 2024 revenue:
$1.009B

>11,200
employees worldwide

Culture of innovation
more than 20 significant new products in last 3 years

26
global development centers

Nasdaq: CDNS; S&P 500 and Nasdaq 100 indexes

Source: Cadence Earnings Press Release, April 22, 2024
https://www.cadence.com/en_US/home/company/newsroom/press-releases/pr-ir/2024/cadence-reports-first-quarter-2024-financial-results.html

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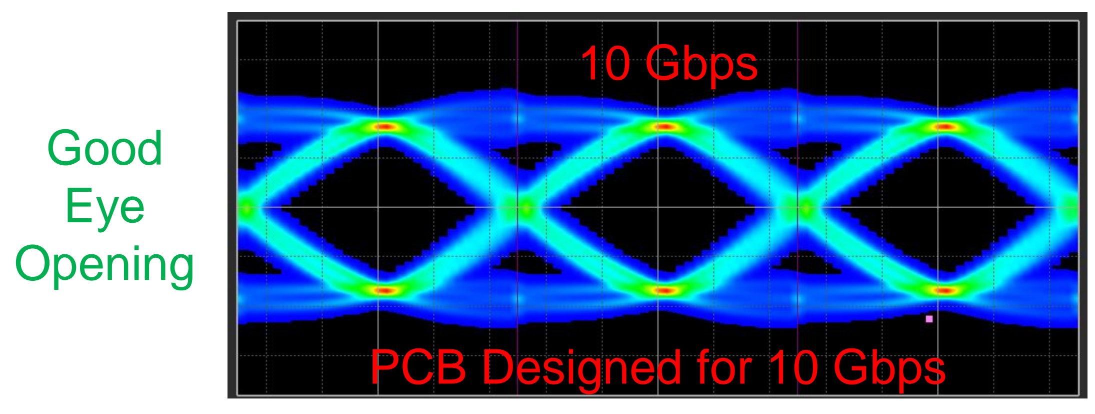
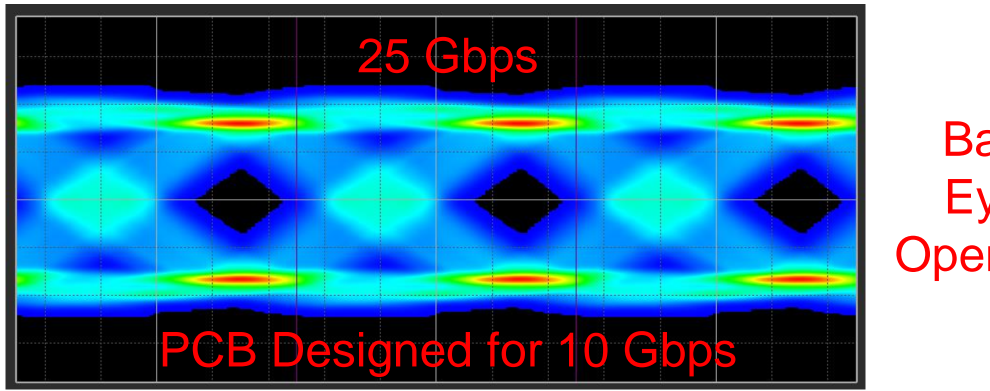
How Does 25Gbps Differ from 10Gbps?

Good Eye Opening





Bad Eye Opening

- Signal, Power, and Thermal Integrity become much more challenging at 25Gbps
- Fast rise times and higher data rates ⇒ interconnects become transmission lines
- Power Distribution Network (PDN) needs to support low voltage and high current
- Increased power dissipation leads to higher junction temperatures, thermal hot spots

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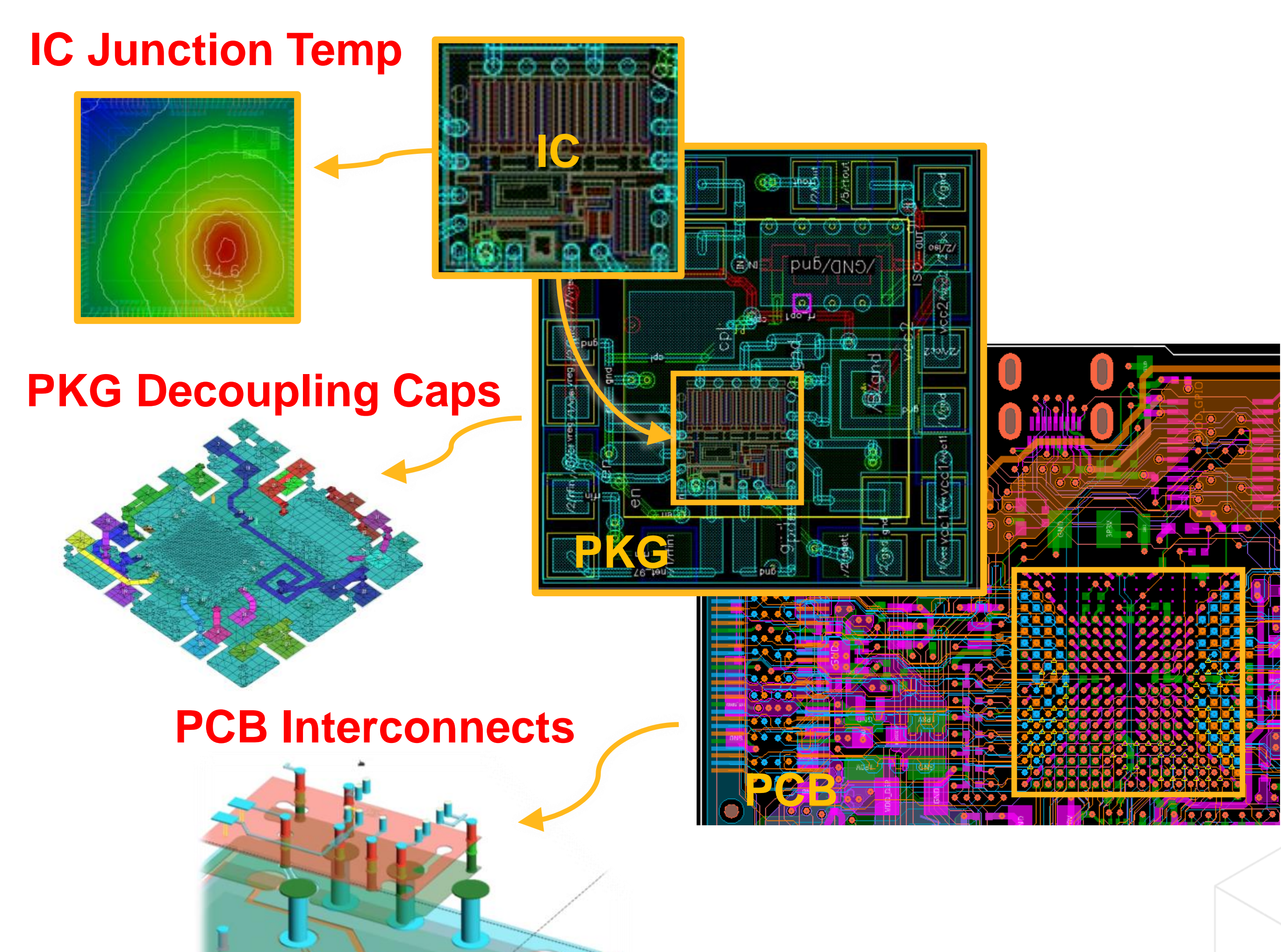
Where can Power, Thermal, and SI Issues Exists in IC, Pkg, PCB?

- At high-speeds need to consider routing at all levels: IC, PKG, PCB
- Fast data rates means higher power, increased current densities and higher temperatures
- Minimize loop inductance with decoupling capacitors at the package
- Optimize signal routes, via structures, return paths, PDN on PCB



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IC Power Optimization Has to Be Full Flow

Optimize Power

Design Creation
High Level Synthesis

Physical Aware logic synthesis
RTL Optimization
RTL Synthesis

Physical Implementation
Implementation System

Signoff
Static Timing Analysis
Signoff Power Analysis

Complete Power Savings Flow

Power Architecture & Optimization

- Multi-power domains
- CPF/UPF support
- RTL power signoff
- Activity driven Mapping & Opto

Power Optimization

- GigaPlace Power-driven placement
- GigaOpt Power-driven optimization
- CCOpt Clock power savings
- NanoRoute Power-driven routing

Power Integrity

- Grid optimization
- IR-based implementation
- Power/signal EM fixing
- Sign Off Voltus power analysis

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Thermal Basics – 3 Modes of Heat Transfer

Package influences
- Package materials
- Package structure
- Package dimensions
- Heat spreader

Chip influences
- Chip area
- Heat generation (hot spots)
- Power consumption

Operating environment influences
- Cooling conditions
- Structure of mounting printed wiring board
- Mounting density
- Ambient temperature

Radiation:
Heat transfer through the emission of the electromagnetic waves

Convection:
Heat transfer from a solid to a fluid, and a phenomenon in which heat moves throughthe fluid

Conduction:
Heat transfer by which heat passes through a material
The vibrations of the molecules in a lattice, or the transportation by free electrons

Convection
Conduction
Radiation

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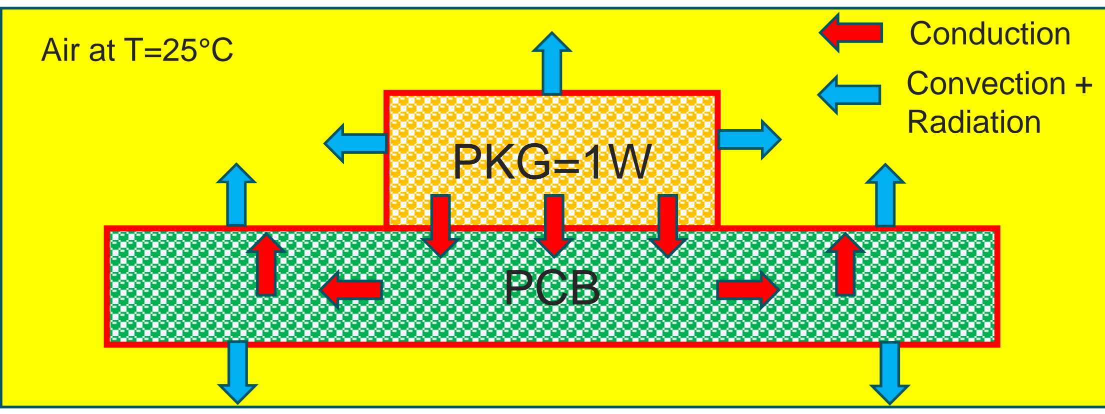
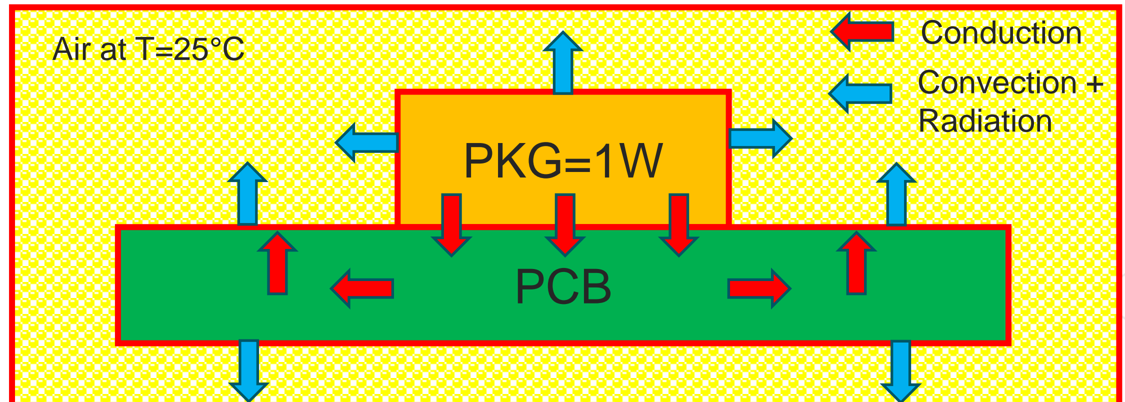
Thermal Basics – FEA vs. CFD

- **FEA (Finite Element Analysis)**: in the context of thermal, it is used to solve conduction problems within solids in detail with convection and radiation effect taken into account in a simplified manner with a boundary condition of heat transfer coefficient.
  - FEA allows detailed and accurate conduction analysis
  - FEA simplifies convection and radiation with a boundary condition with a heat transfer coefficient (no actual simulation of a fluid)



- **CFD (Computational Fluid Dynamics):** in the context of thermal, it is used to solve conduction in a simplified manner (typically) and convection and radiation in detail by actual simulation of fluid flow (e.g.) fan blowing air over a PCB)
  - CFD allows conduction analysis with simplified structures typically.
  - CFD does the actual detailed simulation of convection and radiation. There is no boundary condition of heat transfer coefficient



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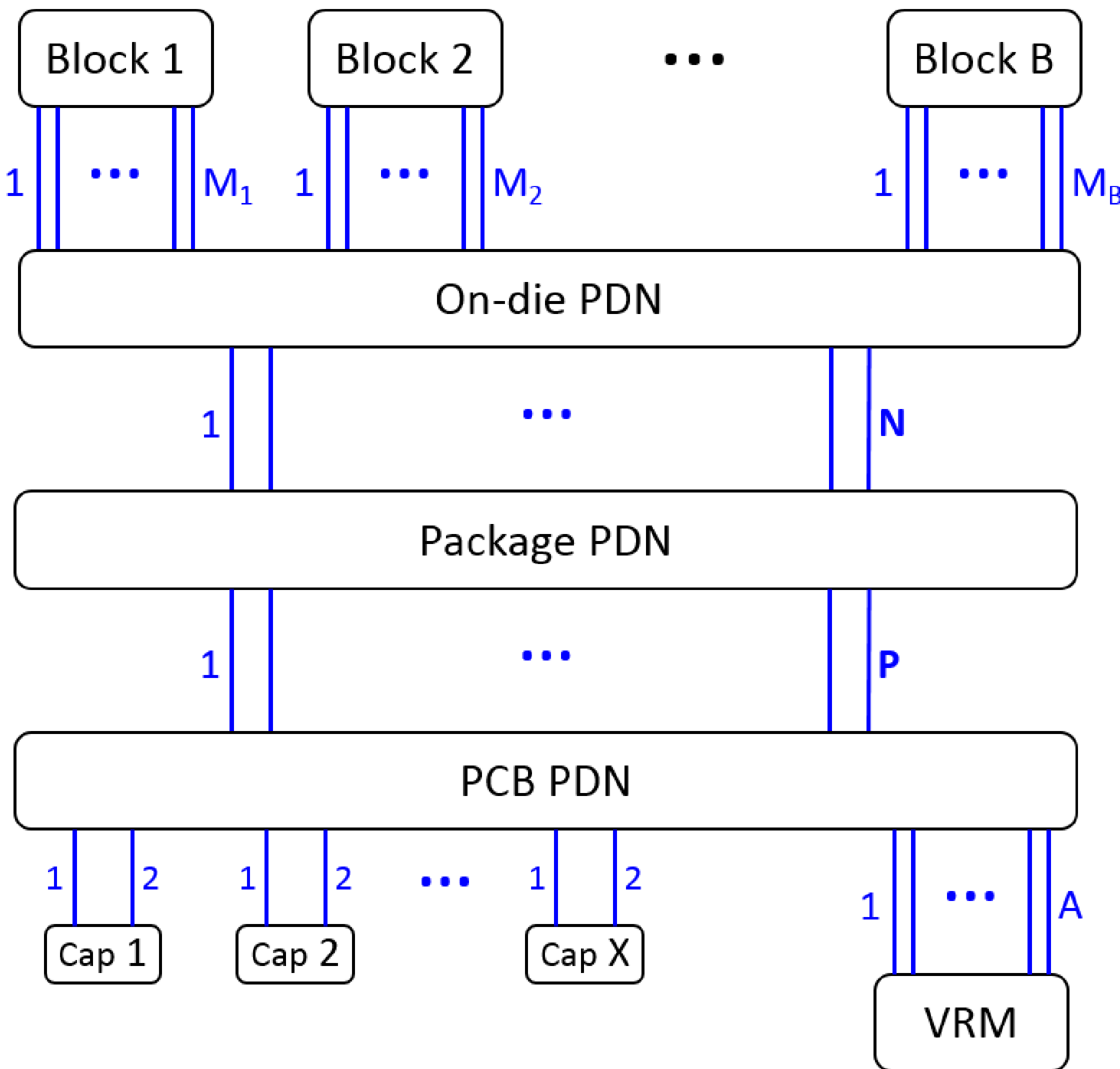
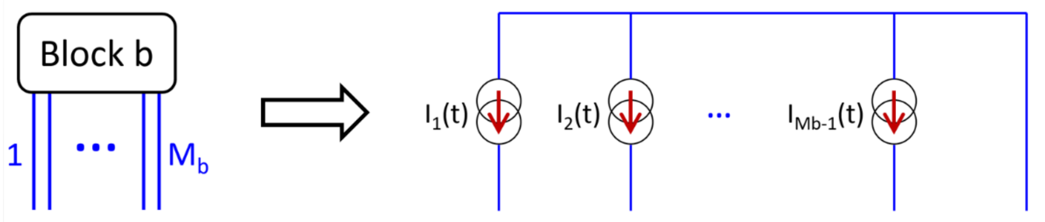
What Power Distribution Network (PDN) Does Your Chip See?





- “Clean” power comes into PCB
- Travels through multiple levels of parasitics
- Non-ideal power delivered to chip

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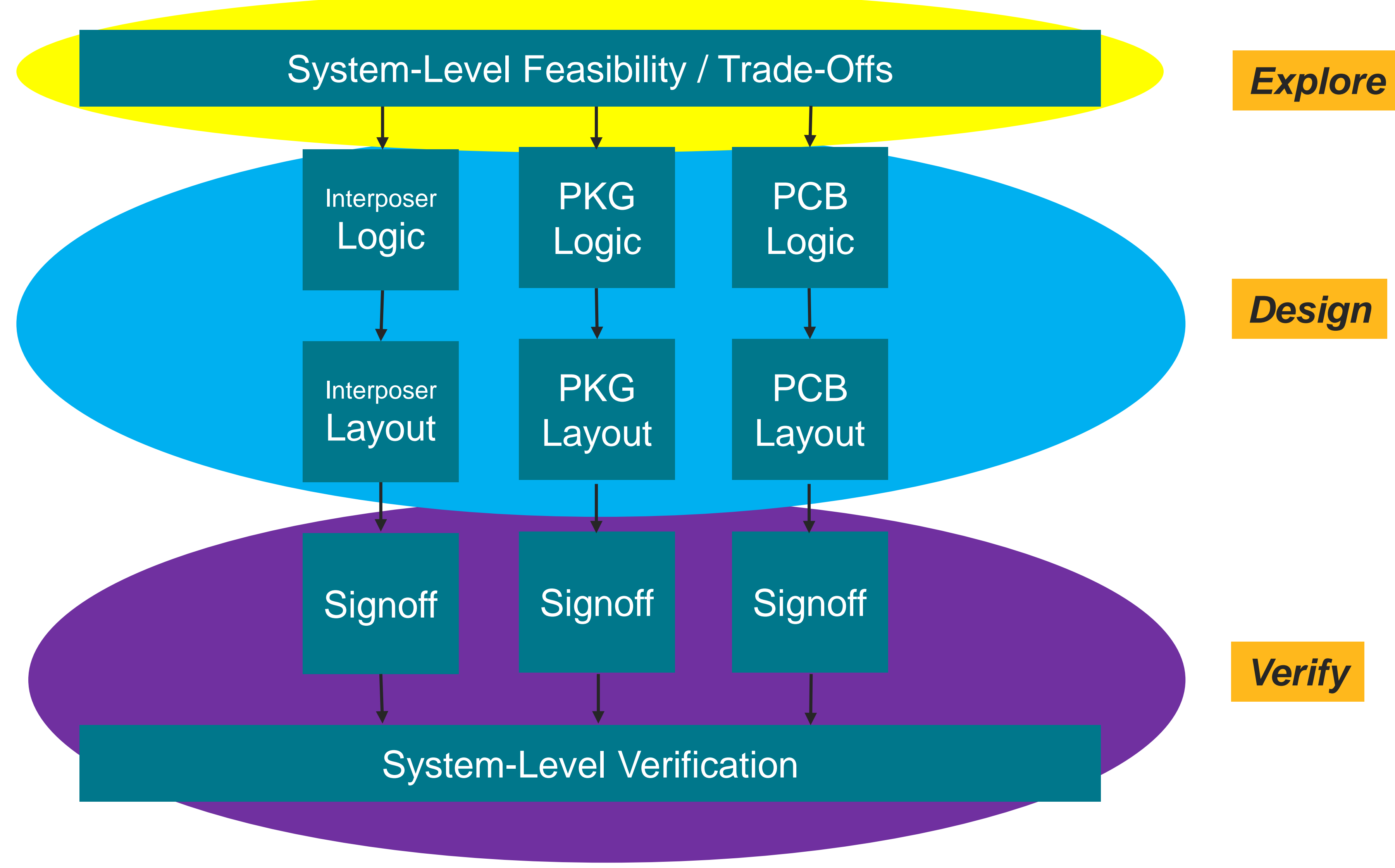
How do you address this? Multiple levels to consider …



Explore

Design

Verify

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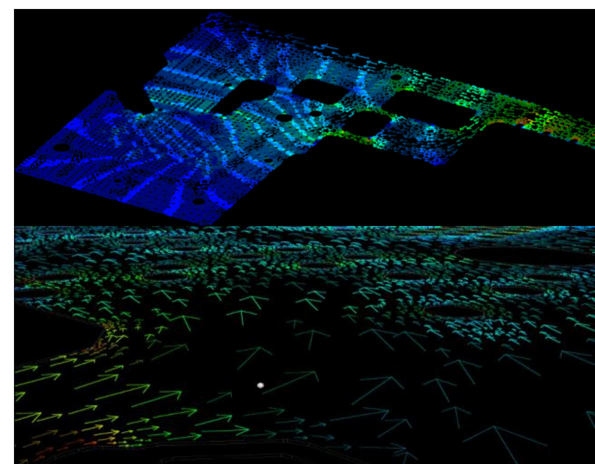
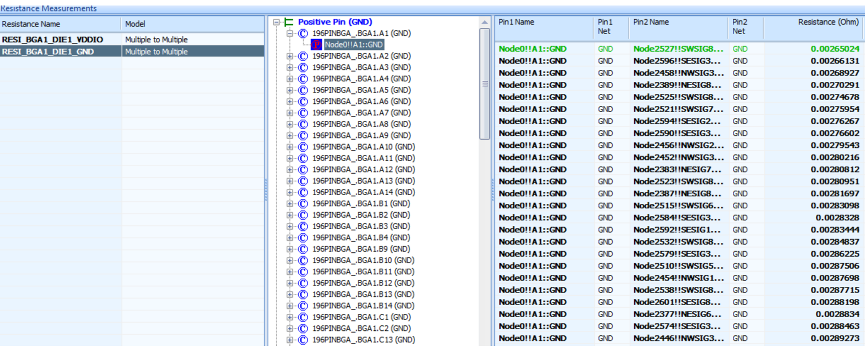
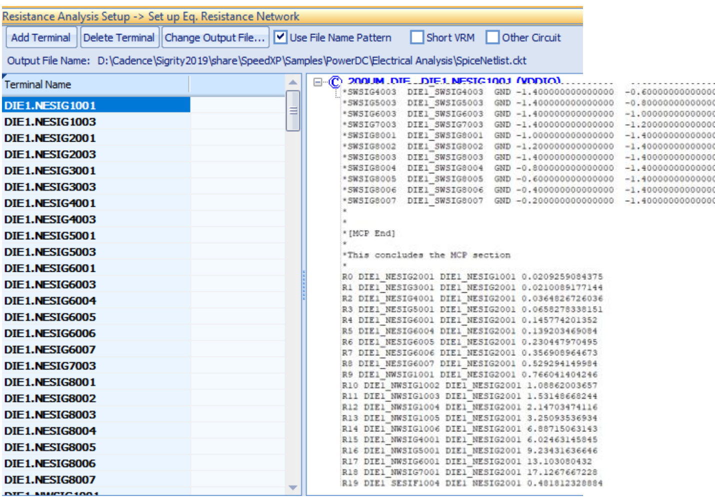
IR Drop Analysis of Package / PCB



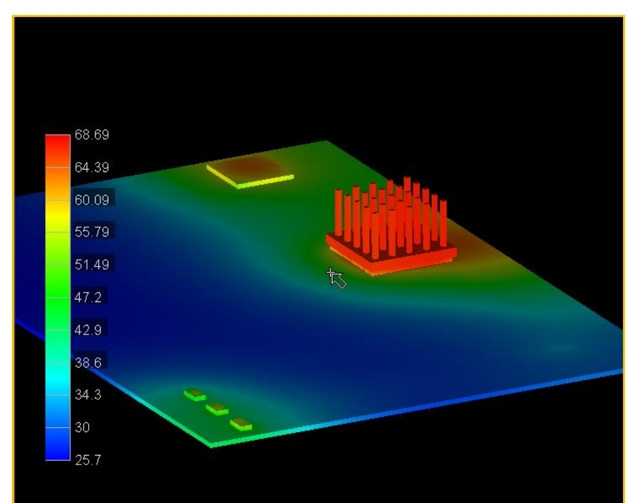
IR Drop Analysis



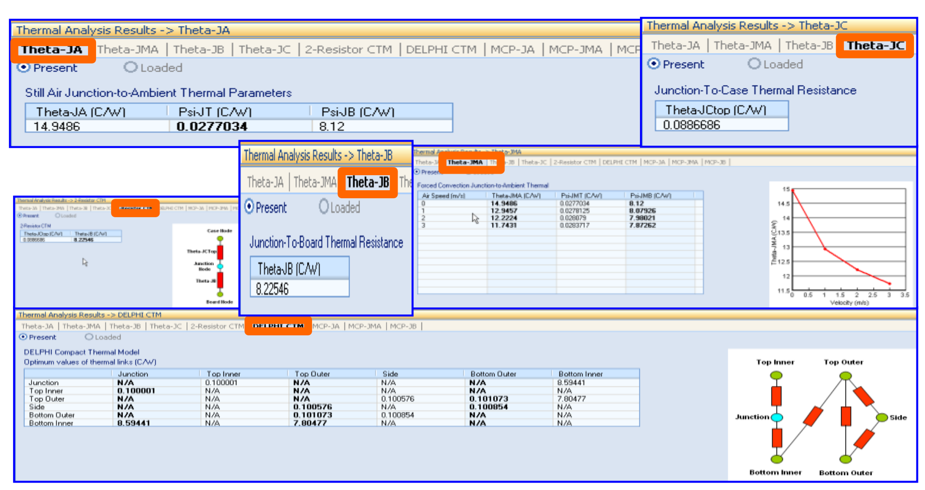
Resistance Measurement



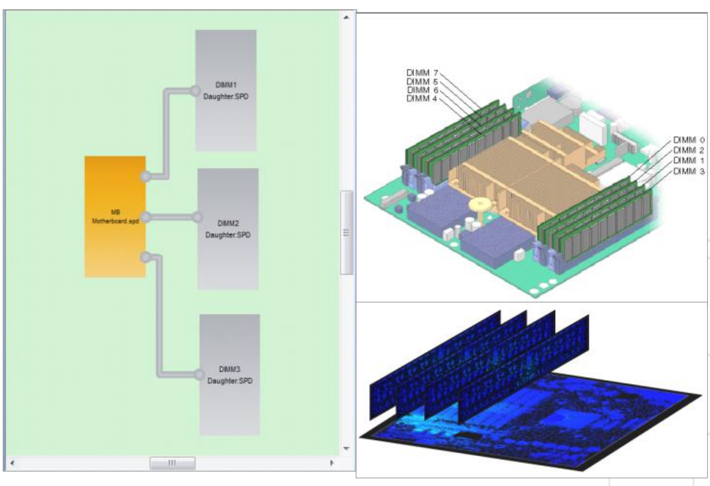
Resistance Network Generation



E/T Co-Simulation



Thermal Model Extraction



Multi-Board Analysis

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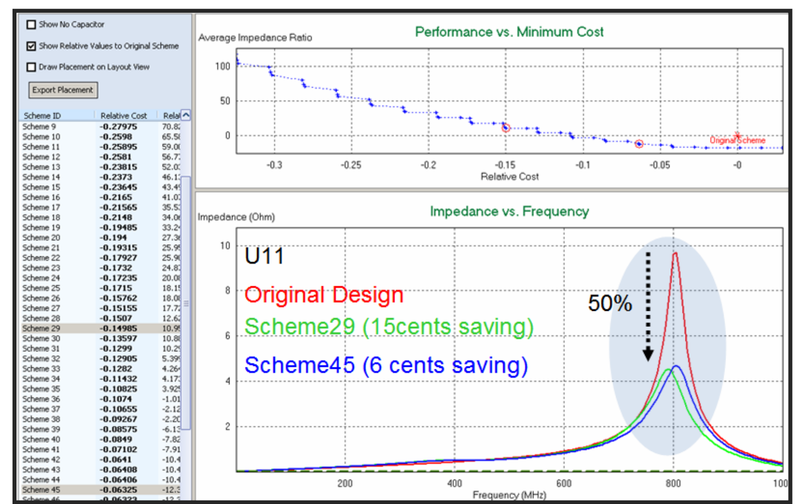
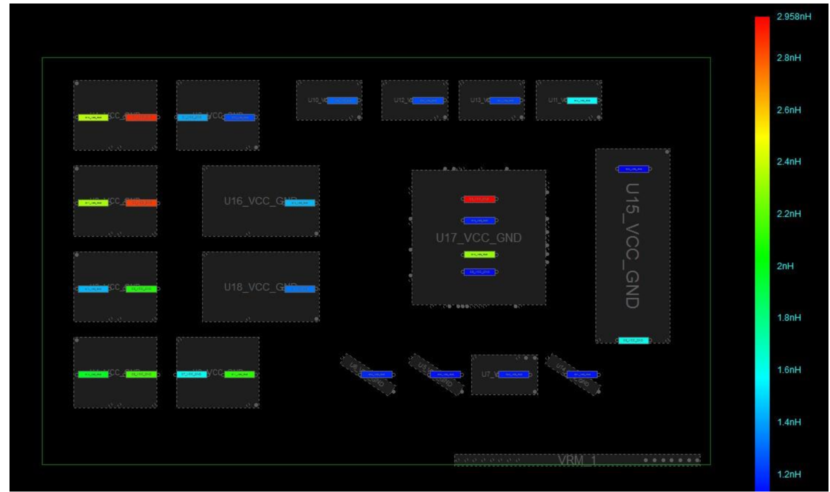
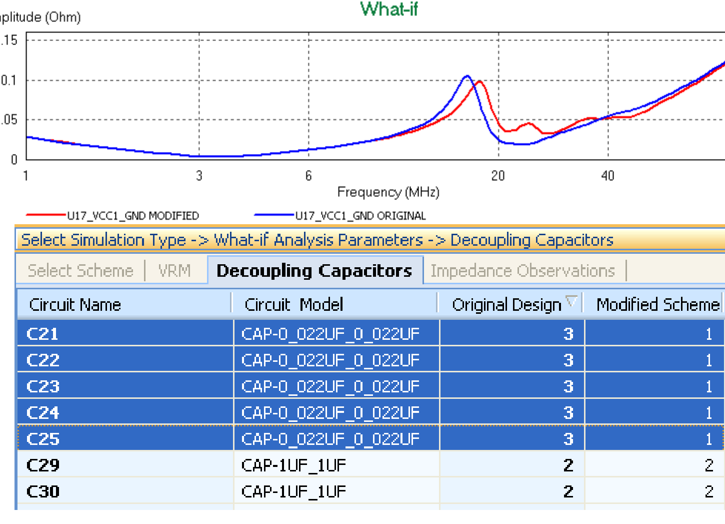
AC Analysis of Package / PCB



Pre- and Post-Layout Optimization

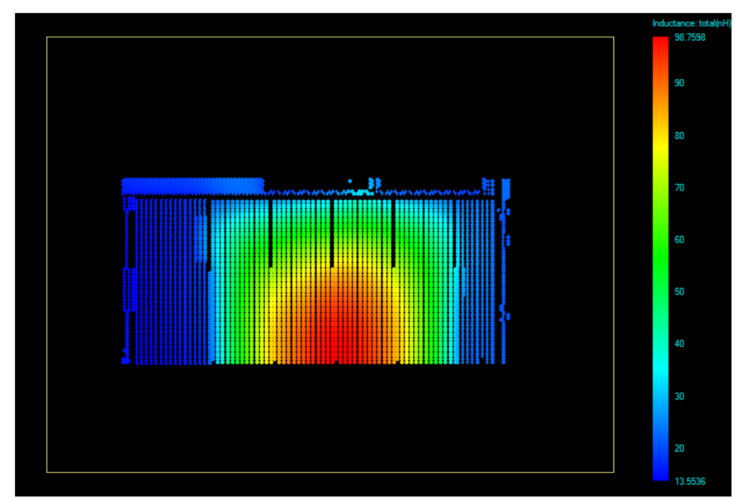


Decoupling Capacitor Loop Inductance

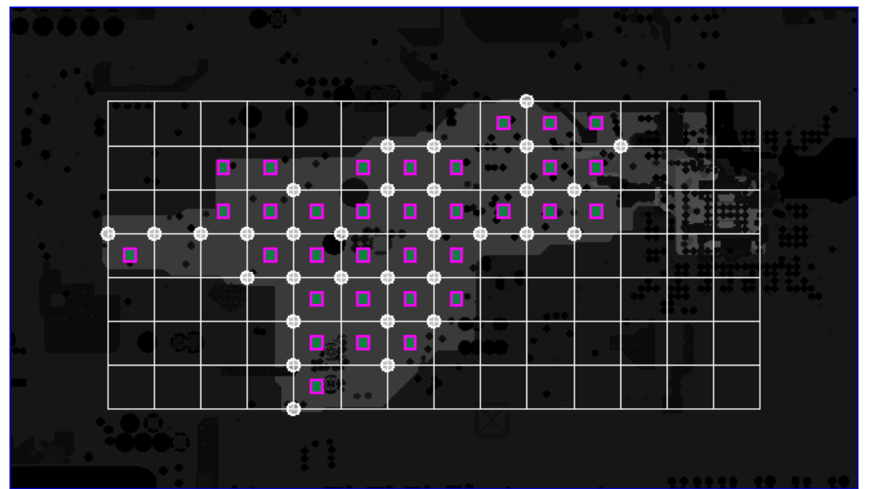


Circuit Name	Circuit Model	Original Design	Modified Scheme
C21	CAP-0_022UF_0_022UF	3	1
C22	CAP-0_022UF_0_022UF	3	1
C23	CAP-0_022UF_0_022UF	3	1
C24	CAP-0_022UF_0_022UF	3	1
C25	CAP-0_022UF_0_022UF	3	1
C29	CAP-1UF_1UF	2	2
C30	CAP-1UF_1UF	2	2

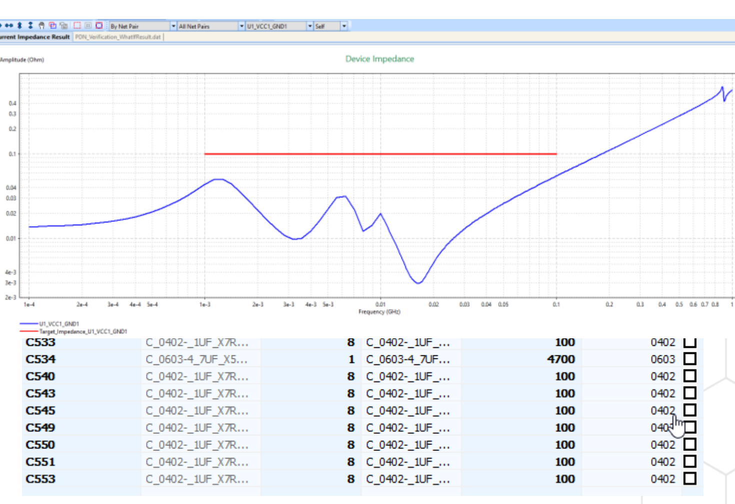
What-if Analysis



IC Device Power Pin Inductance



EMI Capacitor Optimization



PDN Impedance Check

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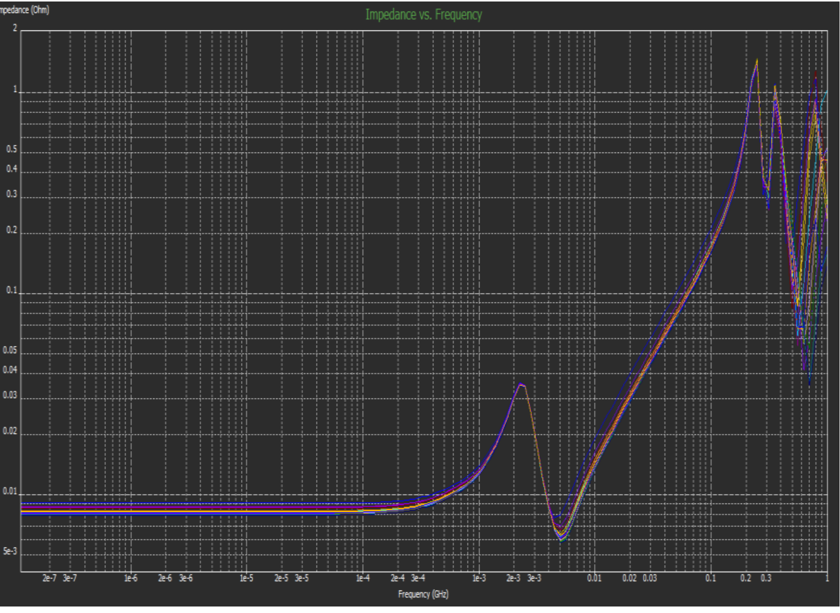
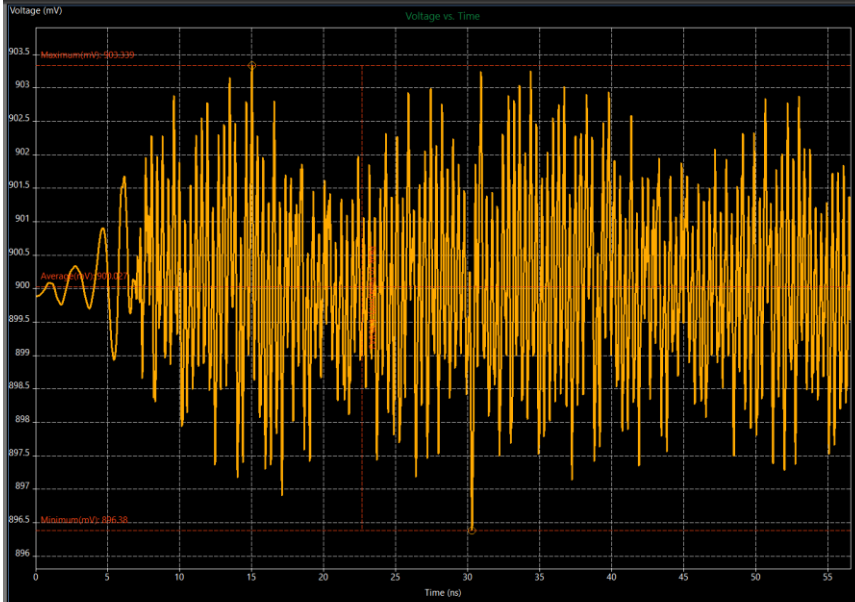
System-Level PI Analysis

- Put packages and PCB(s) all together for complete PDN
- Check frequency domain vs. target impedance
- Check time domain vs. ripple spec

VRM
PCB
SnP
PKG
IC0
IC1
IC2
IC3
IC4
IC5
IC6
IC7





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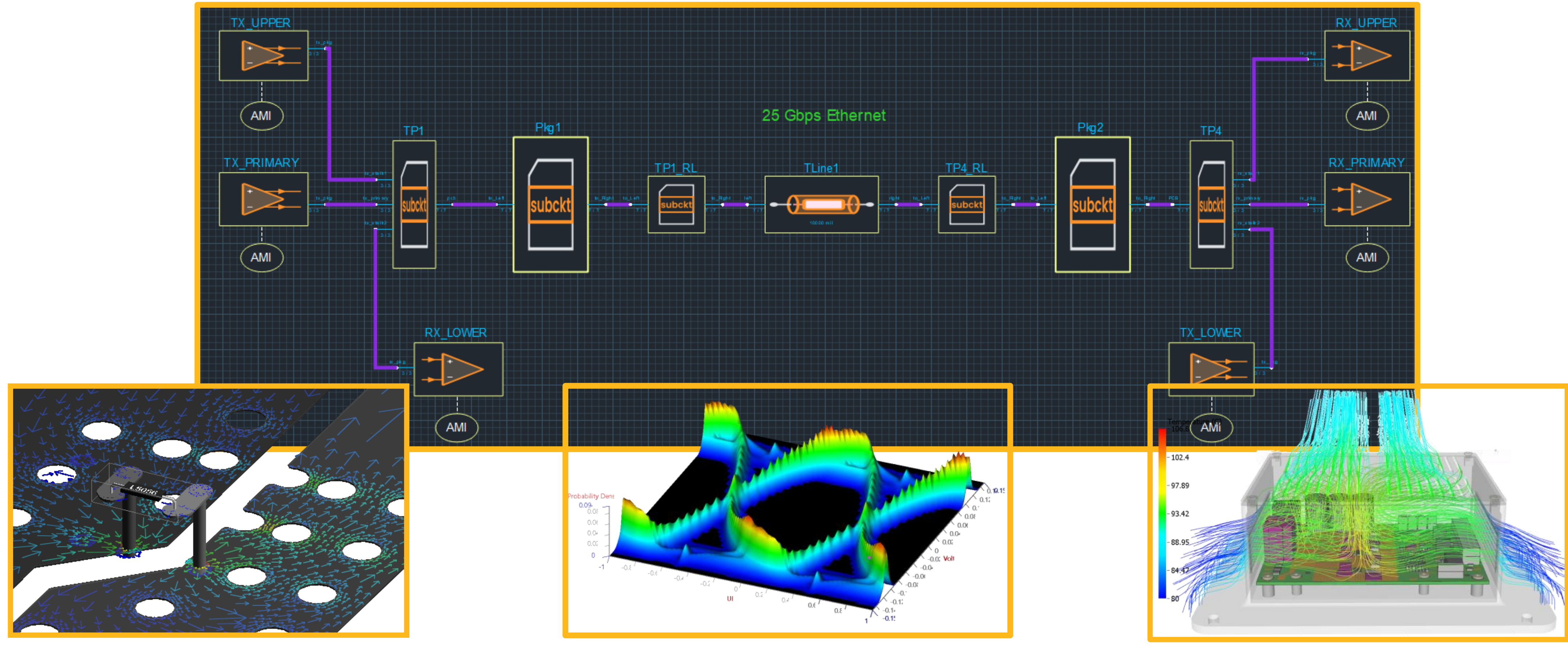
Cadence MSA Technology Enables High-Speed Operation



Power Integrity

Operate at low supply voltages
Eliminate high current density spots
Meet PDN AC impedance

Signal Integrity

Optimized Signal/Return-path routing
Minimize reflections and crosstalk
Validate System Compliance

Thermal Integrity

Guarantee Junction Temperatures
Eliminate thermal hot spots
Optimize system cooling

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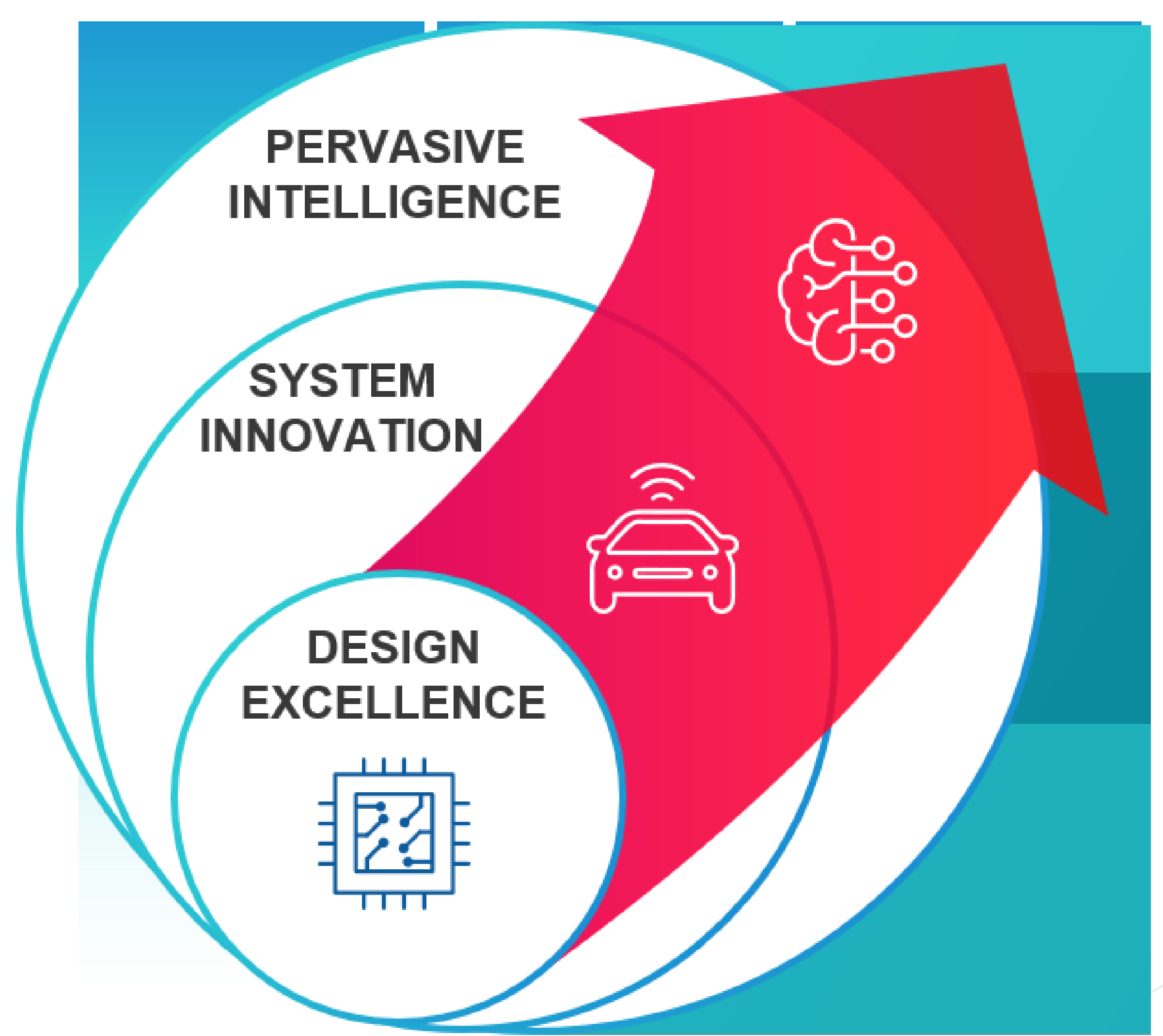
Staying Cool Summary

- Signal, Power, and Thermal Integrity become much more challenging at high-speeds
- Fast data rates means higher power consumption, increased current densities, and higher temperatures must be considered in the design process
- High-speed signal routes, via structures, return paths must be designed with transmission lines and modeled with electromagnetic extractions
- The complexity of high-performance systems design is an iterative, resource intensive, and expensive process that can benefit from AI driven analysis
- Cadence offers the complete solution of design platforms, multi-physics analysis engines, and is now bringing AI to bear on the system design problem



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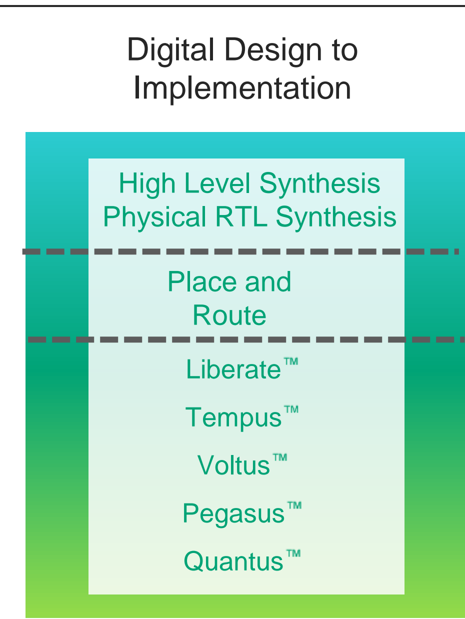
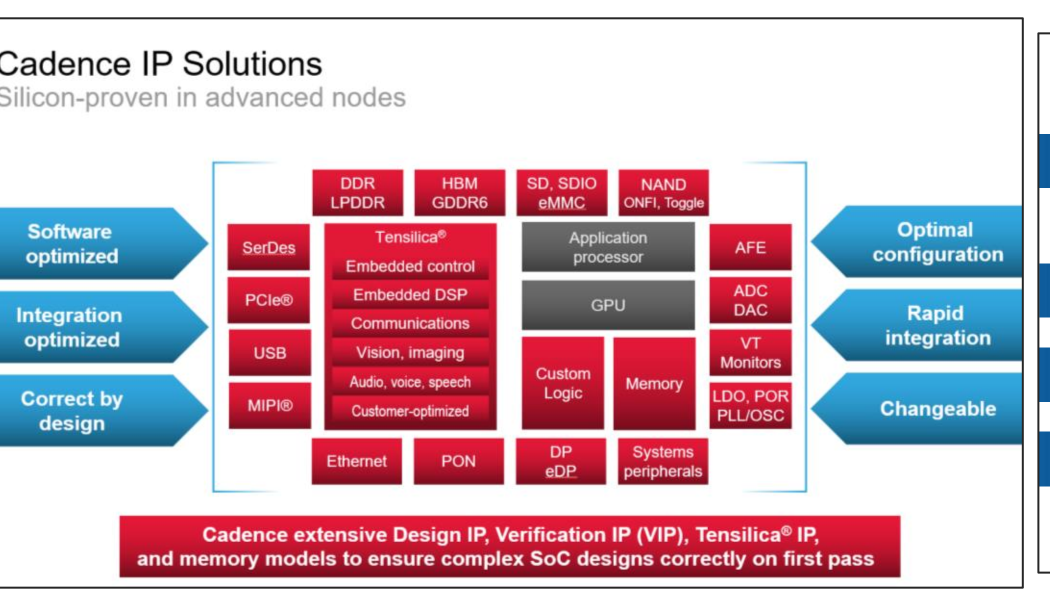
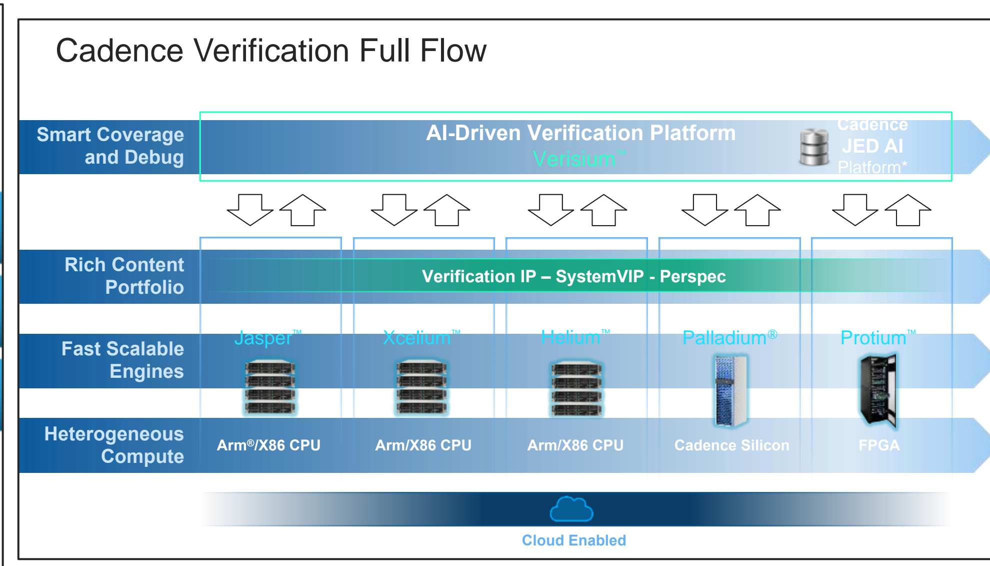
Cadence: HFT Accelerator Partner

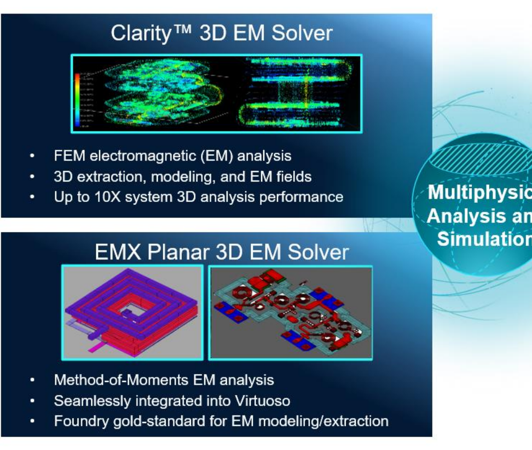
Contact us:
hft@cadence.com

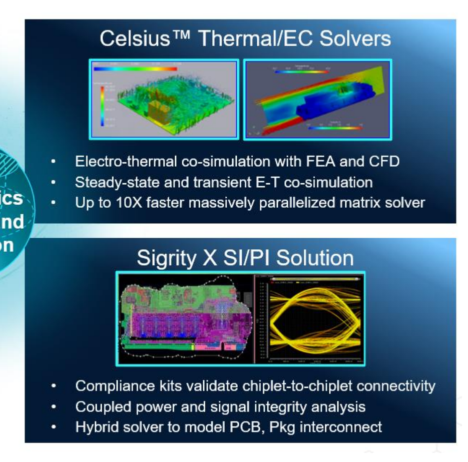




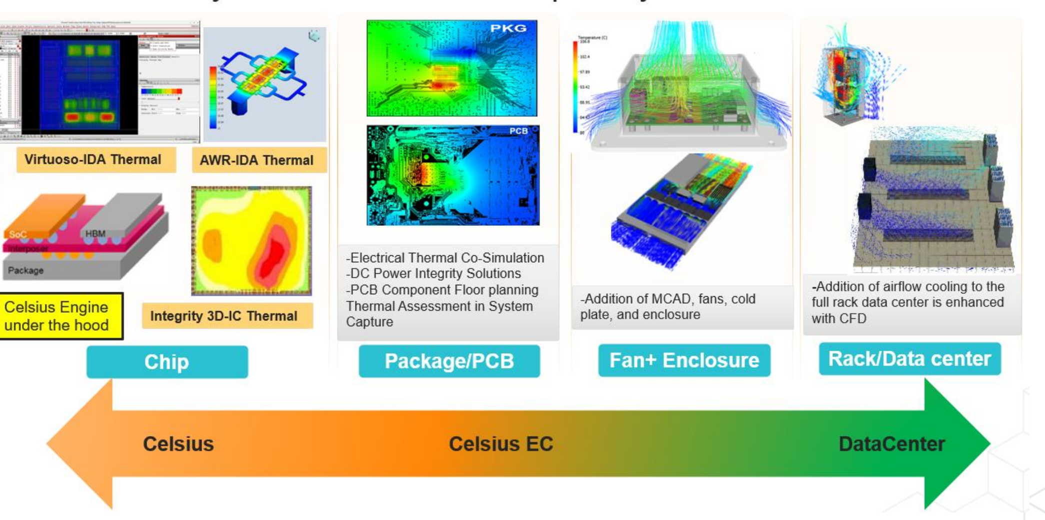


Cadence Multiphysics Simulation and Analysis Technology





Thermal Analysis Solutions from Chip to Systems



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