Open-Source Pros & Cons in the FPGA Development Flow

Stephen Kopec
Senior FAE Manager, Data Center Global Technical Sales
AECG, AMD

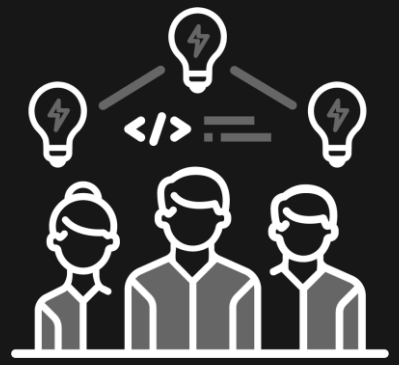
What is Open-Source Software?

Publicly Accessible

Anyone can see the code, modify, and distribute as needed

Collaborative Development

Relies on peer review and community production

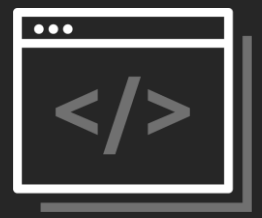


Widely Distributed

Becomes more widely distributed based on demand

For many years, engineers have relied on open-source software for various end-products

Does Open-Source Apply to FPGA Designs?



RTL (VHDL, Verilog, SystemVerilog) can be used as open-source

- Differs from software due to restrictions in silicon architecture / device
- If RTL is made generic (inferred RTL, not instantiated), success rate increases

In many FPGA designs (e.g., FinTech), low latency takes priority

- Requires meticulous design, placement, and routing

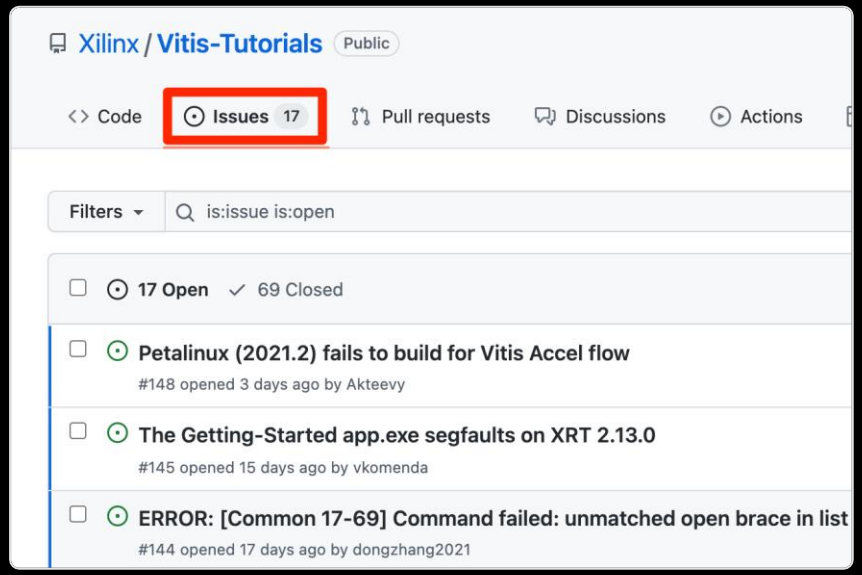
Where can AMD add value to this commonly used methodology?

- GitHub used for AMD designs
- Many users collaborate globally to test and verify examples

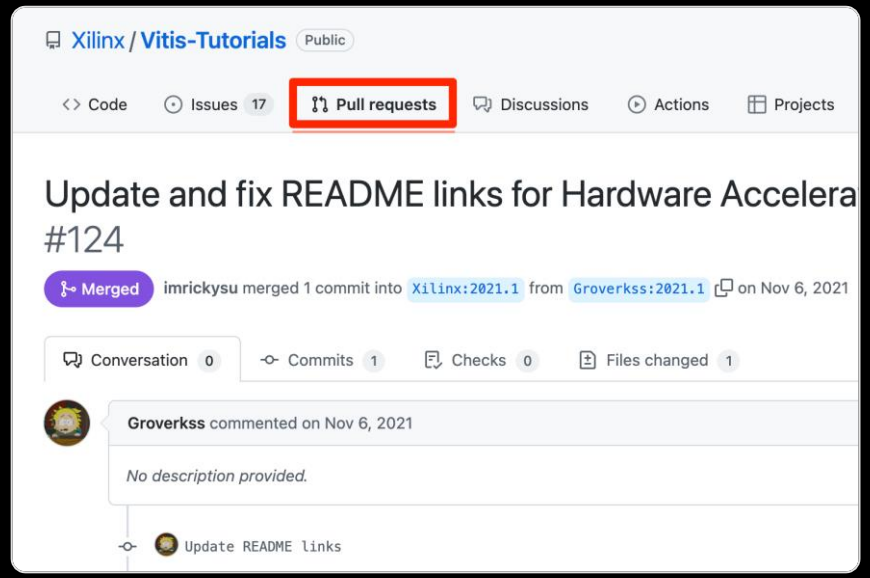
Contribution to GitHub

- AMD has several public GitHub sites
- Example: The Vitis-Tutorials is an open-source project on GitHub
- Contributions to Vitis™-Tutorials are welcome

Report Issues



Send Pull Requests (PR's)
to Fix Bugs or Typos



AMD

Applying Open-Source to AMD Products

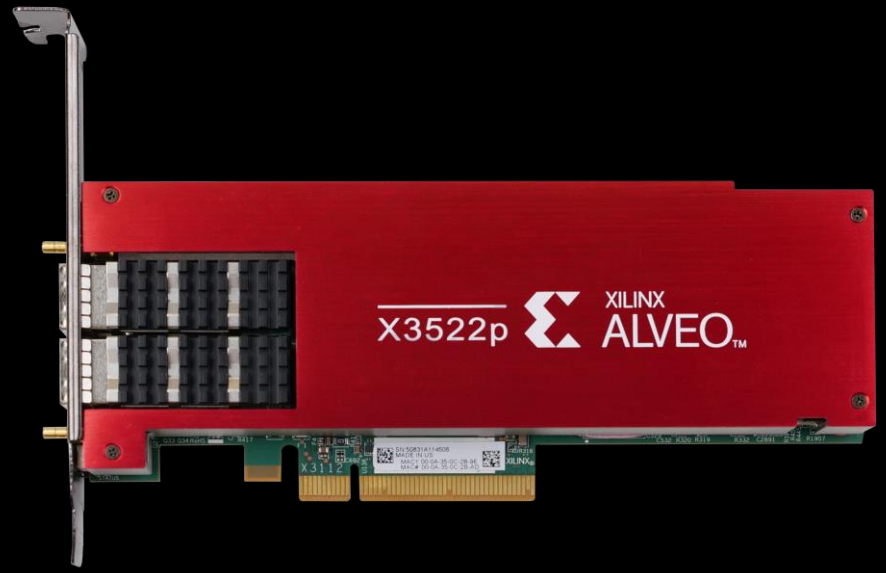
- AMD (AECG, formerly Xilinx) has been providing FPGA products for decades
- More recently, Alveo™ (FPGA-based) accelerator cards focus on data center applications
- Alveo X3522PV, built for Fintech applications, allows users to collaborate on open-source
  - Vitis– SW Developers (HW Acceleration)
  - Vivado – HW Developers (Low Latency)

XILINX VITIS™

Software Developers
Hardware Acceleration

VIVADO™

Hardware Developers
Low Latency




AMD

Disclaimer & Attribution

Timelines, roadmaps, and/or product release dates shown in these slides are plans only and subject to change.

The information contained herein is for informational purposes only and is subject to change without notice. While every precaution has been taken in the preparation of this document, it may contain technical inaccuracies, omissions and typographical errors, and AMD is under no obligation to update or otherwise correct this. Advanced Micro Devices, Inc. makes no representations or warranties with respect to the accuracy or completeness of the contents of this document, and assumes no liability of any kind, including the implied warranties of noninfringement, merchantability or fitness for particular purposes, with respect to the operation or use of AMD hardware, software or other products described herein. No license, including implied or arising by estoppel, to any intellectual property rights is granted by this document. Terms and limitations applicable to the purchase or use of AMD's products are as set forth in a signed agreement between the parties or in AMD's Standard Terms and Conditions of Sale.

”Zen,” “Zen 2,” “Zen 3,” “Zen 4,” “CDNA,” “CDNA 2,” “Vega,” “Polaris,” “GCN,” “Naples,” “Rome,” “Milan” and “Genoa” are codenames for AMD architectures and are not product names.