



ÜberNIC™

Your NIC Can't Keep Up With Modern Markets – Ours Can

October 19<sup>th</sup>, 2022



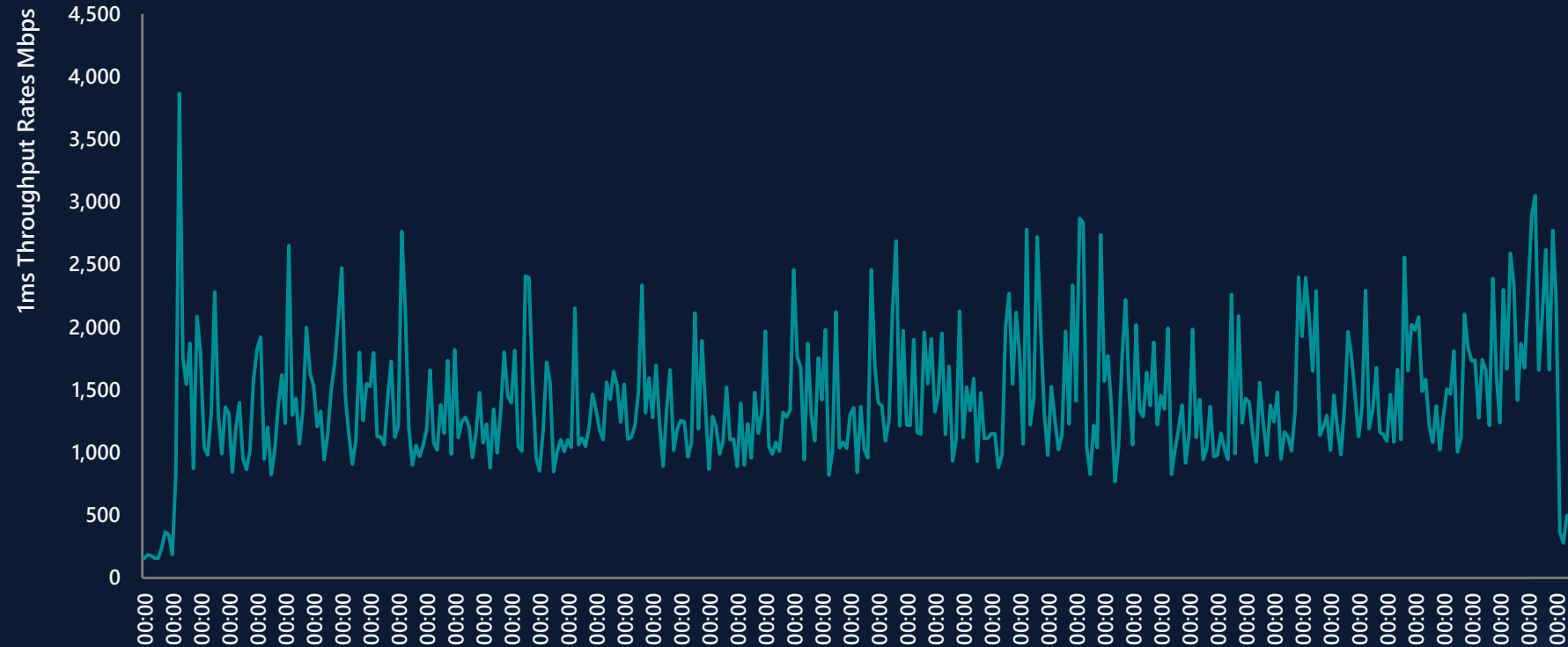
73.2%

Market Data Messages w/Payloads  $\leq$  100 Bytes



# The Real World: Frequent Exchange Microbursts

NYSE Integrated Feed 2022-09-26



Source: <https://marketdatapeaks.net/>

## Can Your NIC & Network Stack Handle Real World Scenarios?



# Why The \$#!&%\$ Are My Orders Not Done?



# The Solution: ÜberNIC™

## ■ Performance

- FPGA-Based NIC Implementing a 100% Hardware Network Stack
- On-Board Memory Enables Highly Performant & Lossless Buffer
- Ultra-Low-Latency & Ultra-High-Throughput in a Single Package
- Sockets-Compliant, Highly-Optimized PCIe Transfer and Kernel Bypass

## ■ Standards Adherence

- Fully Integrated with Linux Tools (IP, IFCONFIG, ETHTOOL)
- End-User Configuration Preferences (ex: Congestion Control, Retransmit)
- Fully Transparent Disclosure & Documentation

## ■ Extensible

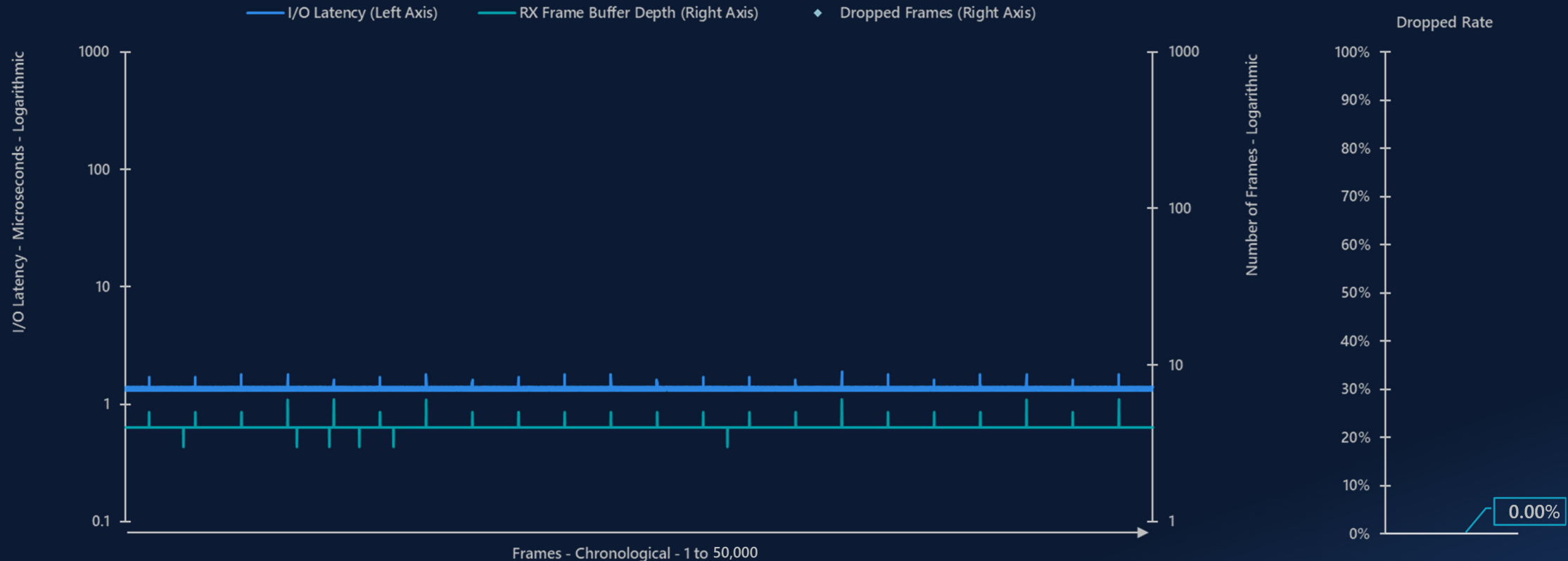
- Timestamping (NTP, PTP, PTP + PPS, FPGA Clock-Counter)
- Internal PCAP
- Market Data Protocol Handler(s)

**Extremely Deterministic, Ultra-Low-Latency & Ultra-High-Capacity**



# The Real World: Meet ÜberNIC™...

## ÜberNIC™ (PCIe Gen 3) @2000Mbps Constant Throughput Rate



Not a STAC Research Benchmark

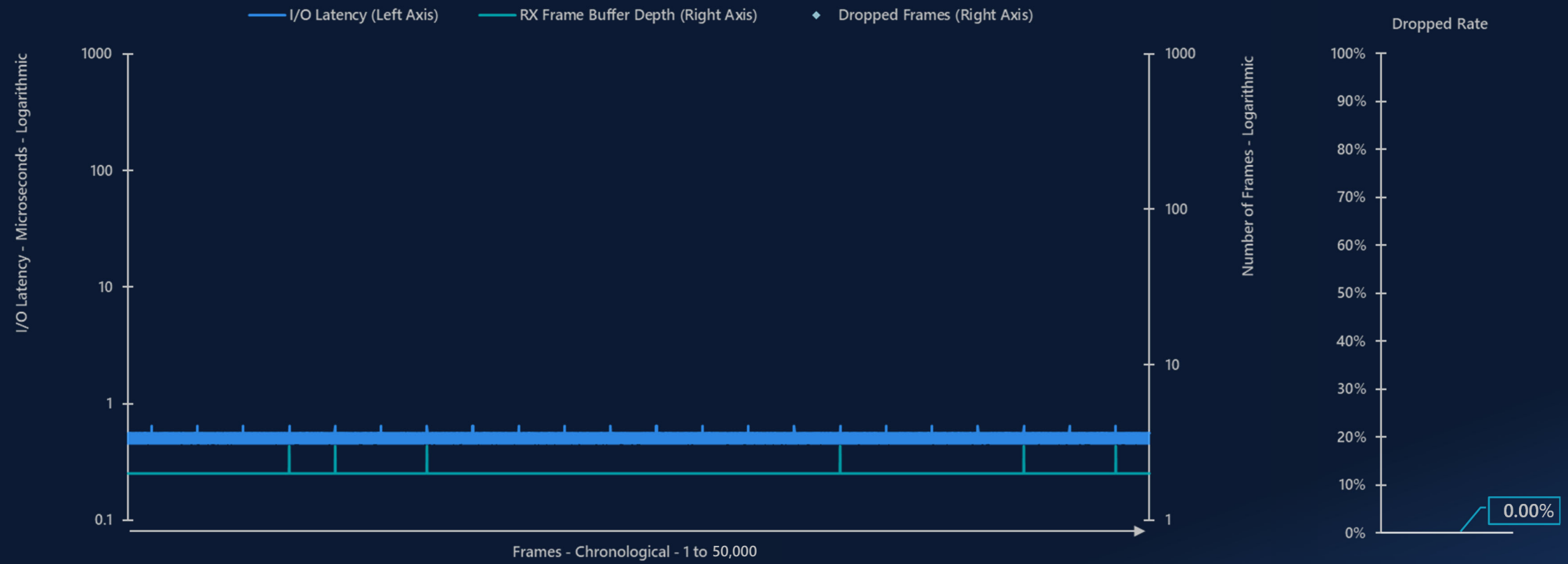
Pre-Production Intel Agilex I-Series Tested By Naros.TaSR™

50,000 Frames | 64B UDP Payload (110B Frame) | Transceiver to Transceiver L2 SOF to SOF via Linux User-Space | Excluding Business Logic



# The Real World: Meet ÜberNIC™...

## ÜberNIC™ Ultra (CXL) @2000Mbps Constant Throughput Rate



Not a STAC Research Benchmark

Pre-Production Intel Agilex I-Series Tested By Naros.TaSR™

50,000 Frames | 64B UDP Payload (110B Frame) | Transceiver to Transceiver L2 SOF to SOF via Linux User-Space | Excluding Business Logic





# The Real World: Meet ÜberNIC™...

## 95<sup>th</sup> Percentile 600Mbps to 2750Mbps Latency Spread

ÜberNIC™

5.03%

600Mbps: 1.35μs; 2750Mbps: 1.42μs

ÜberNIC™ Ultra

1.76%

600Mbps: 0.57μs; 2750Mbps: 0.58μs

Not a STAC Research Benchmark

Pre-Production Intel Agilex I-Series Tested By Naros.TaSR™

50,000 Frames | 64B UDP Payload (110B Frame) | Transceiver to Transceiver L2 SOF to SOF via Linux User-Space | Excluding Business Logic

- Entire Network Stack in Hardware
- FPGA Board Designed For FSI
- CXL for Unimagined Performance



Contact LMS or Your Intel Representative to Learn How ÜberNIC™ Solves Your Data Latency & Ingestion Problems

**Sample Boards Available January 2023**

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