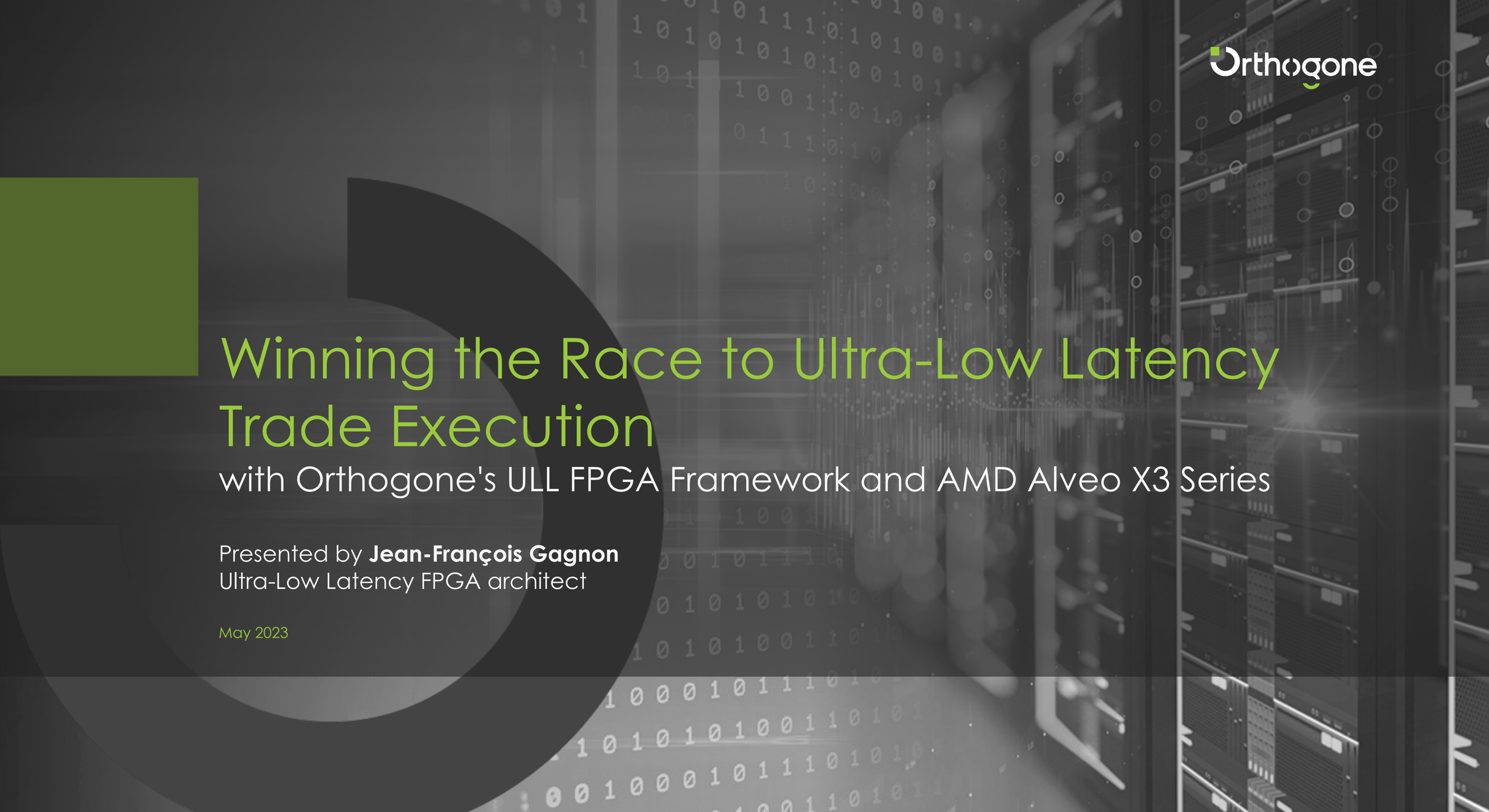


Orthogone

Winning the Race to Ultra-Low Latency Trade Execution

with Orthogone's ULL FPGA Framework and AMD Alveo X3 Series

Presented by **Jean-François Gagnon**
Ultra-Low Latency FPGA architect

May 2023

FPGA IP Solutions Offering

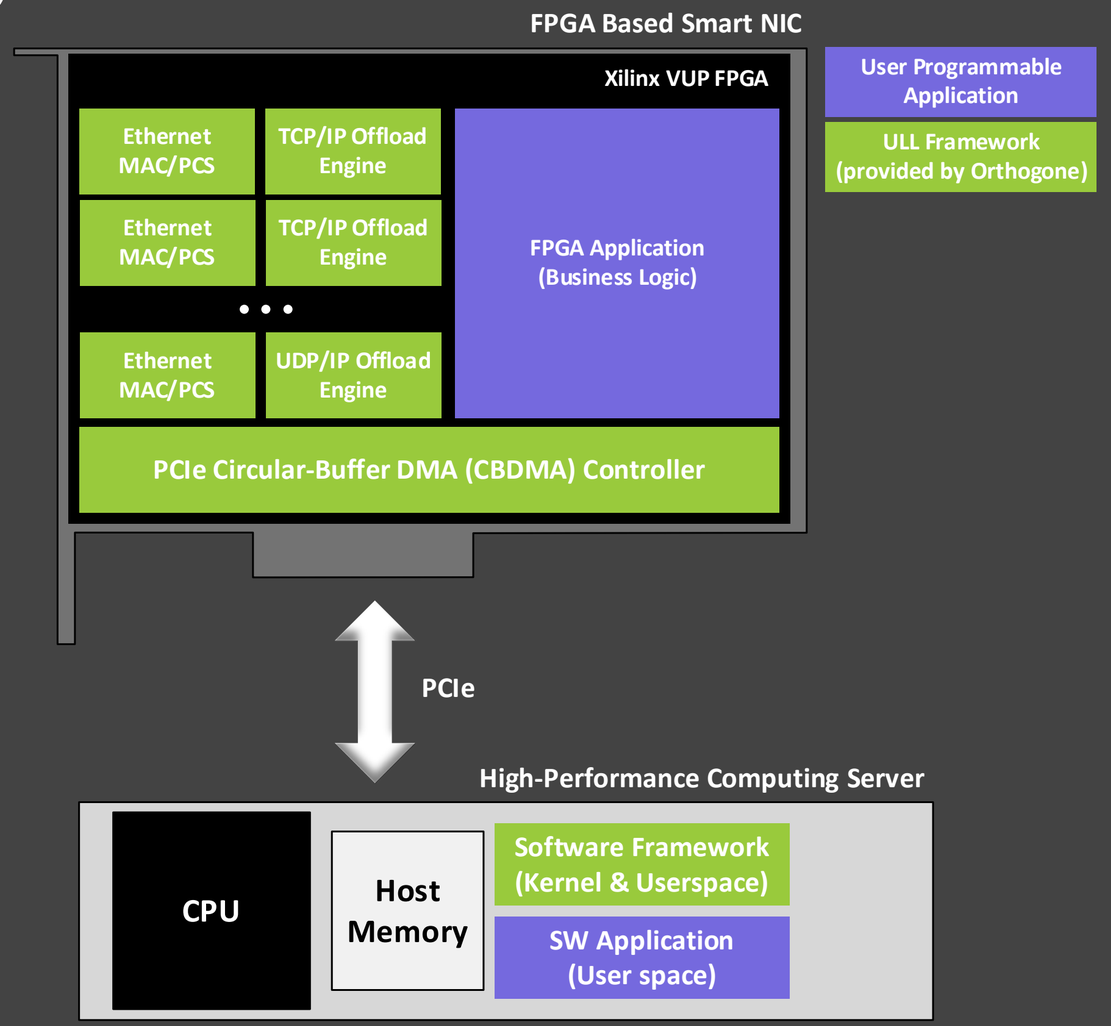
ULTRA-LOW LATENCY NETWORKING SOLUTIONS

ULL FPGA Framework(FDK)

- Best-in-class FPGA and SW solution to develop reconfigurable applications that require ultra-low latency performances.
- Designed explicitly for trading applications
- Full suite of ULL FPGA IP cores
- FPGA Dev kit (design & simulation environment, reference design examples, debug tools, etc.)
- SW Framework (drivers, API, debugger, etc.)

ULL FPGA IP Cores

- Ethernet MAC/PCS (1 – 100G) with opt. RS-FEC
- TCP/IP Offload Engine
- UDP/IP Offload Engine
- PCIe Streaming DMA Controller



ULL FPGA Framework(FDK) Key Features

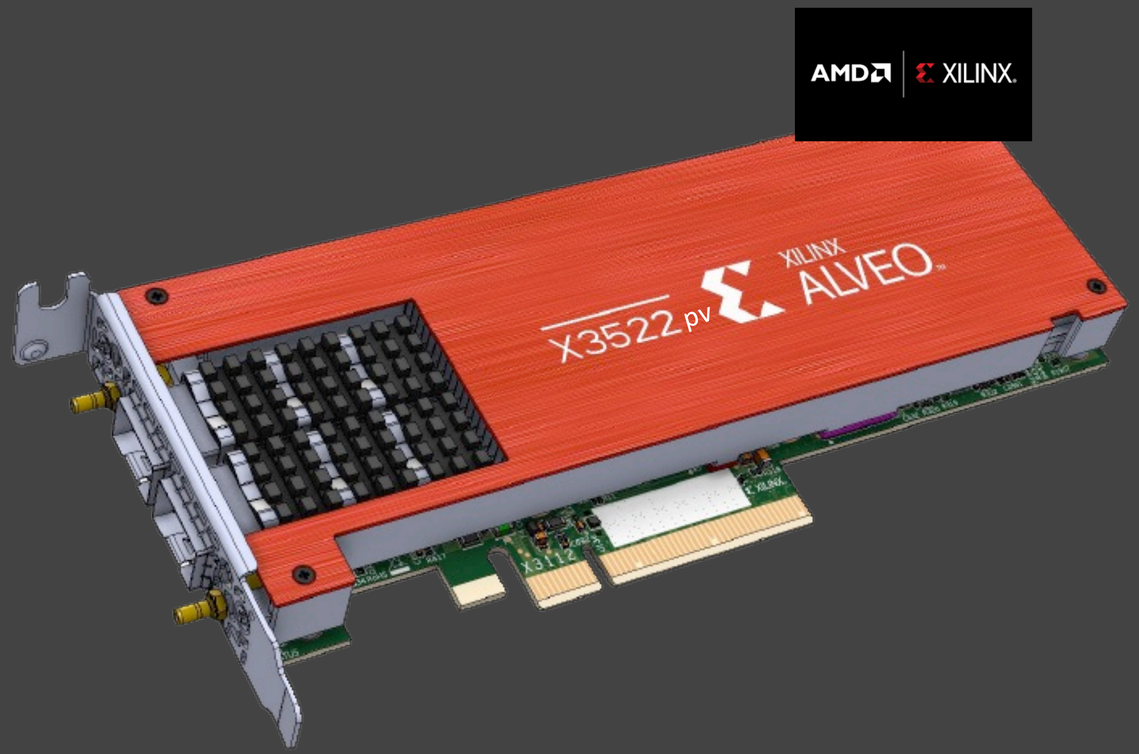
- Optimized explicitly for financial use cases
- Highly flexible and configurable FPGA development platform to support multiple applications
- Typical FPGA resources utilization < 15%
  - *(4 ports TCP/UDP, 32 sessions/port)*
- *Three Alveo reference designs are provided:*
  - *Complete Financial solution*
  - *ULL-MAC/PCS*
  - *ULL-CBDMA*
  - *Includes a detail User Guide document*

- **Highly parametrizable cores**, e.g.:
  - MAC/PCS SERDES Width / Speed
  - Number of sessions & number of ports
  - PORT protocol (TCP,UDP or direct MAC)
  - TCP/IP, UDP/IP Mode: S/F, Cut-through
  - DMA: Number of Interfaces, number of queues per interface, size of queues, etc.

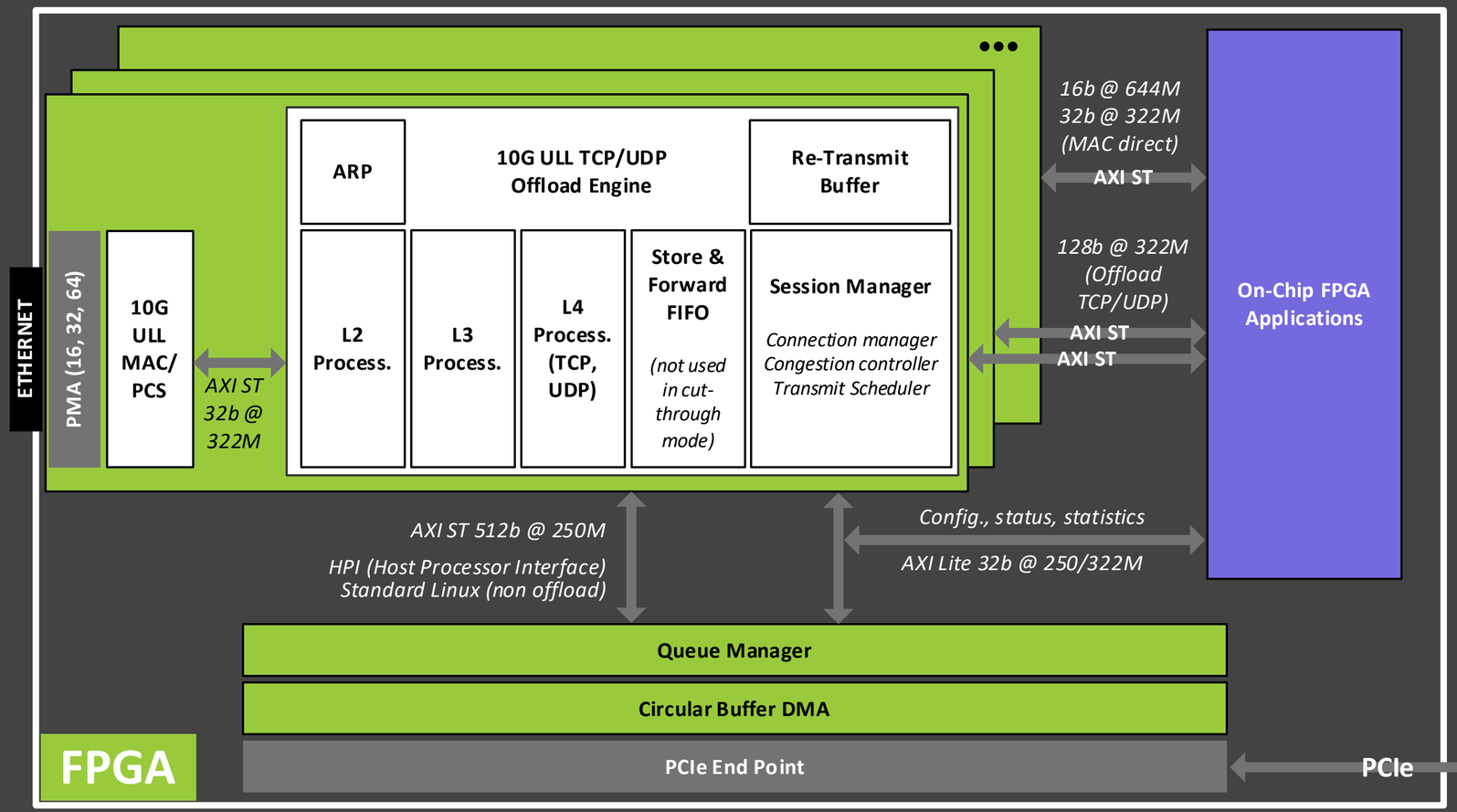
ULL FPGA Framework(FDK) Hardware Platforms

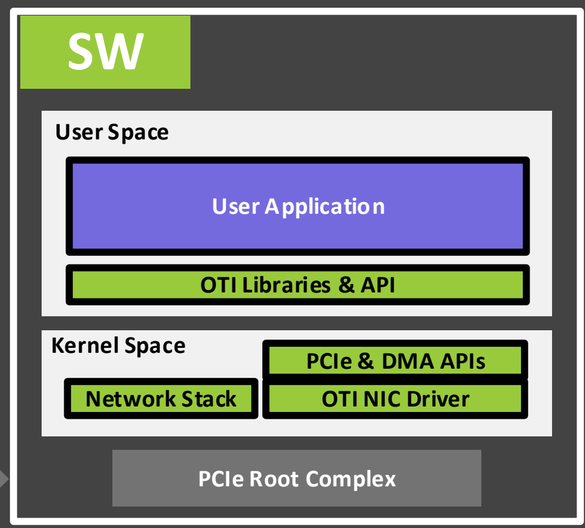
AMD x3522pv

- 4x10/25 GE
- Single slot, half-length, half-height
- PCI Express ® Gen 4 x8 / Gen 3 x8
- Up to two 4GB DDR4 (72b with ECC at 2400MT/s)
- Distributed RAM / BRAM / UltraRAM (14.2Mb / 74.3Mb / 99Mb)
- FPGA: XCUX35-3VSVA1365E
- 16b SERDES @ 644MHz (GTY)
- Speed Grade: -3



ALVEO Complete Finance Solution Ref design





- **Standard AXI-4 Interfaces**
  - 1G ULL MAC (644/322/250MHz)
  - 10G ULL Processing at 644/322MHz
  - 25G ULL Processing at 644/402MHz
- **Offload Engines :** Store-Fwd, Cut-Through
- **MAC/PCS SERDES:**
  - 1G / 10G: 16b or 32b
  - 25G: 64b (40b)
- **Host Processor Interface (HPI)** to support non-offload protocols with standard Linux

ULL FPGA Framework Performances

NOT STAC BENCHMARKS

ULL 10G MAC/PCS

16b PMA / 16b AXI-4 (644MHz)

- Tx**SoP** to Rx**SoF** (no Rx Async FIFO)
  - MAC/PCS = 4.7ns
  - GTY = 15.6ns
  - **Total = 20.3ns**

- Tx**SoP** to Rx**SoP** **(including Rx Async FIFO, including PREAMBLE)**
  - MAC/PCS= 18.6ns
  - GTY = 15.6ns
  - **Total = 34.2ns**

    (including Rx CDC, including PREAMBLE)

Notes:

- *Rx**SoF**: Internal signal driven by MAC_Rx and is pre-CDC (first bits of preamble detected)*
- *Tx**SoP** and Rx**SoP**: TMAC first valid to RMAC first valid (first bits of MAC DA)*

ULL 10G TCP/IP

Two operating modes

- **Store & Forward (S/F):** TxFIFO used to compute TCP Payload size and checksum (Tx), RxFIFO used to drop packets (FCS, TCP checksum errors)
- **Cut-Through (CT):** Bypass TxFIFO and RxFIFO. User must provide pre-computed size and checksum values (Tx).

Cut-Through Mode Mode Latency Performances

- Tx path = 6.2ns
- *The ULL-TCP/UDP Offload Engine transmit latency is measured from the valid signal assertion at the input of ull_top (output of OTI-On-Chip Application) to the valid assertion at the output of ull_top. This is from start of packet to start of packet (SoP to SoP)*
- Rx path = 46.5ns; Latency excluding headers reception = 6.2ns
- *All Rx latency numbers for ULL-TCP/UDP Offload engine are measured after headers removal. The first byte of the packet after headers removal is called Start of Payload. In TCP, 54 bytes of header @322MHz on a 32-bit data bus is always included in the latency specifications, i.e. all specified latency numbers include 40.3ns latency caused by headers reception for any received packet. The removed headers are Ethernet, IP and TCP/UDP headers.*

ULL FPGA Framework(FDK)
Key Features recap

- Pure FPGA trading solution
- Hybrid trading solution (FPGA+Software)
- ULL-MAC/PCS 16b@644MHz
  & 32b@322MHz
- Already integrated on Alveo x3522pv
- Highly parametrizable to match
  your needs.

- Easy to use, Alveo reference designs
  are provided for each IPs
- HW Platforms supported:
  - Xilinx UltraScale+ FPGA
  - Xilinx Alveo (x3522pv reference design)
  - Xilinx Versal (to be supported)

Orthogone Overview

Developers of the Seemingly Impossible

Orthogone offers highly specialized engineering solutions focused on the design of innovative products requiring in-depth knowledge of software development, embedded systems, FPGA and SoC.

90+
Multidisciplinary R&D Team

2007
Inception

Privately Held
Headquartered in Montreal (Canada)

FPGA
Solutions & IP Cores Technologies

R&D Services

- Systems engineering
- Software development
- Hardware design
- FPGA Design & Verification

Key Industries

- Datacenter & Comms
- Defense & Aerospace

FPGA IP Portfolio

- ULL FPGA Framework
- Ethernet MAC/PCS/FEC
- TCP/IP Offload Engine
- UDP/IP Offload Engine
- PCIe DMA Controller

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