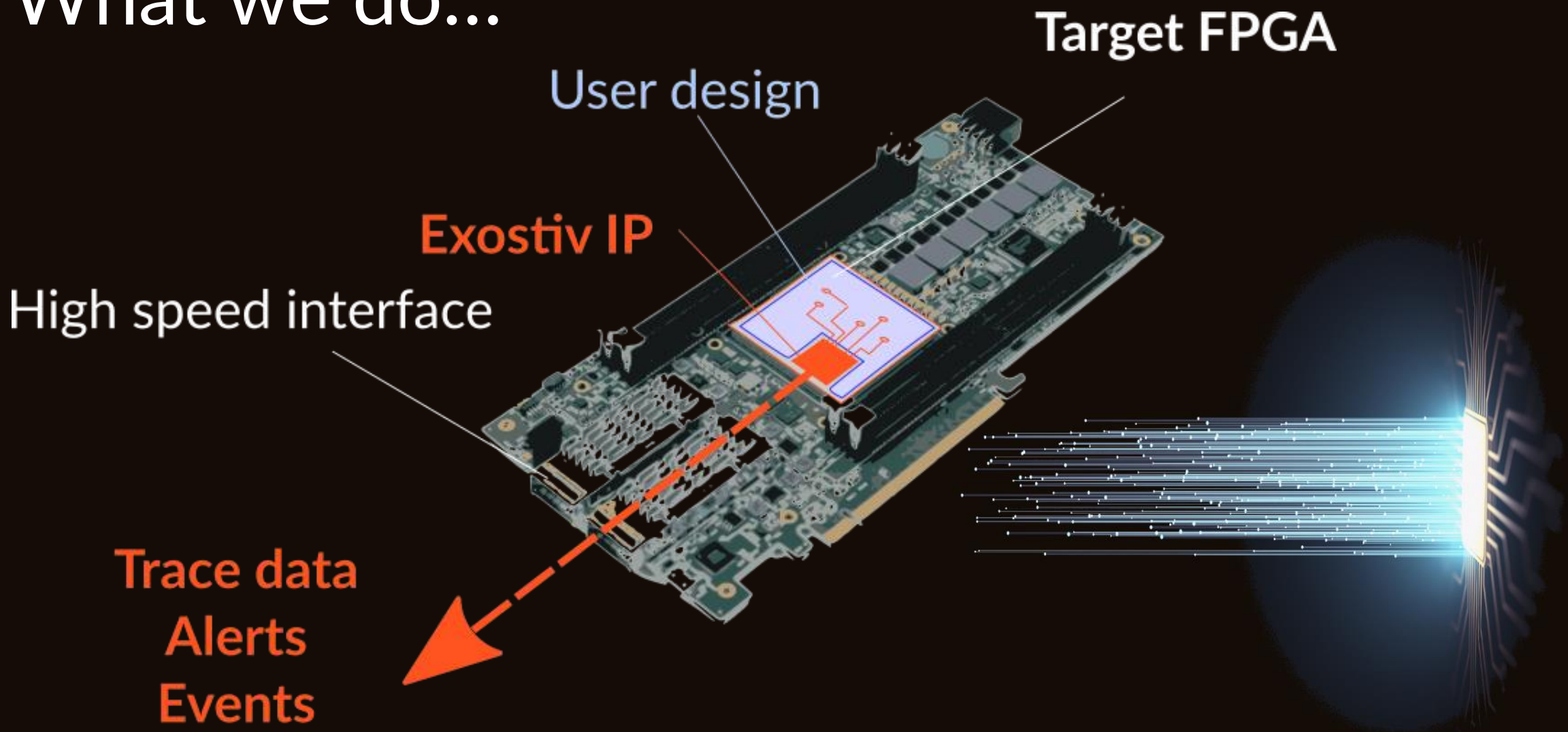
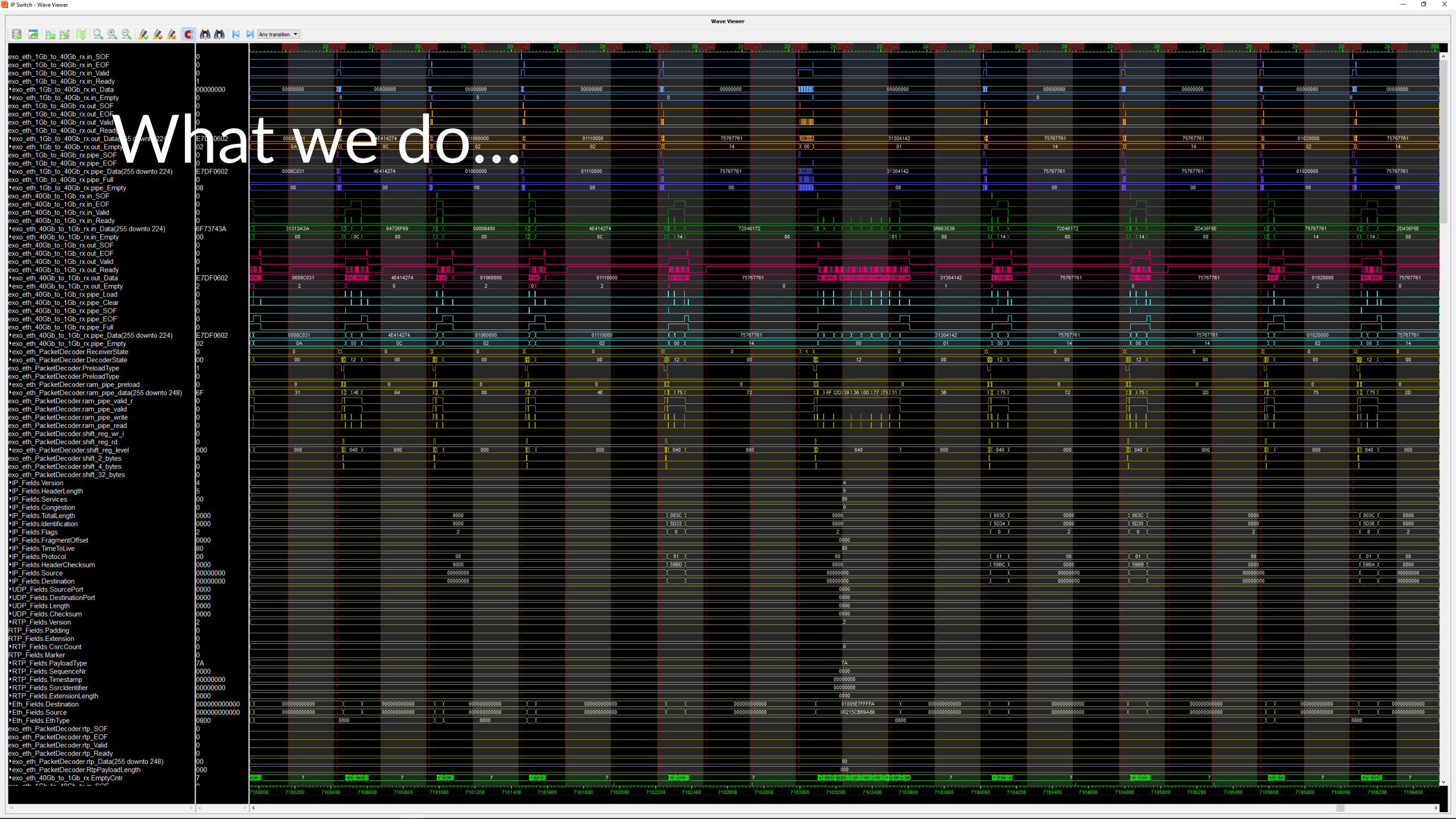
EXOSTIV LABS Visibility into the FPGA.

Do you *really* know what happens inside your FPGA?

EXOSTIV LABS Visibility into the FPGA.

What we do…




IP Switch - Wave Viewer
Wave Viewer
Any transition
What we do...
exo_eth_1Gb_to_40Gb_rx.in_SOF
exo_eth_1Gb_to_40Gb_rx.in_EOF
exo_eth_1Gb_to_40Gb_rx.in_Valid
exo_eth_1Gb_to_40Gb_rx.in_Ready
exo_eth_1Gb_to_40Gb_rx.in_Data
exo_eth_1Gb_to_40Gb_rx.in_Empty
exo_eth_1Gb_to_40Gb_rx.out_SOF
exo_eth_1Gb_to_40Gb_rx.out_EOF
exo_eth_1Gb_to_40Gb_rx.out_Valid
exo_eth_1Gb_to_40Gb_rx.out_Ready
exo_eth_1Gb_to_40Gb_rx.out_Data(255 downto 224)
exo_eth_1Gb_to_40Gb_rx.out_Empty
exo_eth_1Gb_to_40Gb_rx.pipe_SOF
exo_eth_1Gb_to_40Gb_rx.pipe_EOF
exo_eth_1Gb_to_40Gb_rx.pipe_Data(255 downto 224)
exo_eth_1Gb_to_40Gb_rx.pipe_Full
exo_eth_1Gb_to_40Gb_rx.pipe_Empty
exo_eth_40Gb_to_1Gb_rx.in_SOF
exo_eth_40Gb_to_1Gb_rx.in_EOF
exo_eth_40Gb_to_1Gb_rx.in_Valid
exo_eth_40Gb_to_1Gb_rx.in_Ready
exo_eth_40Gb_to_1Gb_rx.in_Data(255 downto 224)
exo_eth_40Gb_to_1Gb_rx.in_Empty
exo_eth_40Gb_to_1Gb_rx.out_SOF
exo_eth_40Gb_to_1Gb_rx.out_EOF
exo_eth_40Gb_to_1Gb_rx.out_Valid
exo_eth_40Gb_to_1Gb_rx.out_Ready
exo_eth_40Gb_to_1Gb_rx.out_Data
exo_eth_40Gb_to_1Gb_rx.out_Empty
exo_eth_40Gb_to_1Gb_rx.pipe_Load
exo_eth_40Gb_to_1Gb_rx.pipe_Clear
exo_eth_40Gb_to_1Gb_rx.pipe_SOF
exo_eth_40Gb_to_1Gb_rx.pipe_EOF
exo_eth_40Gb_to_1Gb_rx.pipe_Full
exo_eth_40Gb_to_1Gb_rx.pipe_Data(255 downto 224)
exo_eth_40Gb_to_1Gb_rx.pipe_Empty
exo_eth_PacketDecoder.ReceiverState
exo_eth_PacketDecoder.DecoderState
exo_eth_PacketDecoder.PreloadType
exo_eth_PacketDecoder.PreloadType
exo_eth_PacketDecoder.ram_pipe_preload
exo_eth_PacketDecoder.ram_pipe_data(255 downto 248)
exo_eth_PacketDecoder.ram_pipe_valid_r
exo_eth_PacketDecoder.ram_pipe_valid
exo_eth_PacketDecoder.ram_pipe_write
exo_eth_PacketDecoder.ram_pipe_read
exo_eth_PacketDecoder.shift_reg_wr_i
exo_eth_PacketDecoder.shift_reg_rd
exo_eth_PacketDecoder.shift_reg_level
exo_eth_PacketDecoder.shift_2_bytes
exo_eth_PacketDecoder.shift_4_bytes
exo_eth_PacketDecoder.shift_32_bytes
IP_Fields.Version
IP_Fields.HeaderLength
IP_Fields.Services
IP_Fields.Congestion
IP_Fields.TotalLength
IP_Fields.Identification
IP_Fields.Flags
IP_Fields.FragmentOffset
IP_Fields.TimeToLive
IP_Fields.Protocol
IP_Fields.HeaderChecksum
IP_Fields.Source
IP_Fields.Destination
UDP_Fields.SourcePort
UDP_Fields.DestinationPort
UDP_Fields.Length
UDP_Fields.Checksum
RTP_Fields.Version
RTP_Fields.Padding
RTP_Fields.Extension
RTP_Fields.CsrcCount
RTP_Fields.Marker
RTP_Fields.PayloadType
RTP_Fields.SequenceNr
RTP_Fields.Timestamp
RTP_Fields.SsrcIdentifier
RTP_Fields.ExtensionLength
Eth_Fields.Destination
Eth_Fields.Source
Eth_Fields.EthType
exo_eth_PacketDecoder.rtp_SOF
exo_eth_PacketDecoder.rtp_EOF
exo_eth_PacketDecoder.rtp_Valid
exo_eth_PacketDecoder.rtp_Ready
exo_eth_PacketDecoder.rtp_Data(255 downto 248)
exo_eth_PacketDecoder.RtpPayloadLength
exo_eth_40Gb_to_1Gb_rx.EmptyCntr

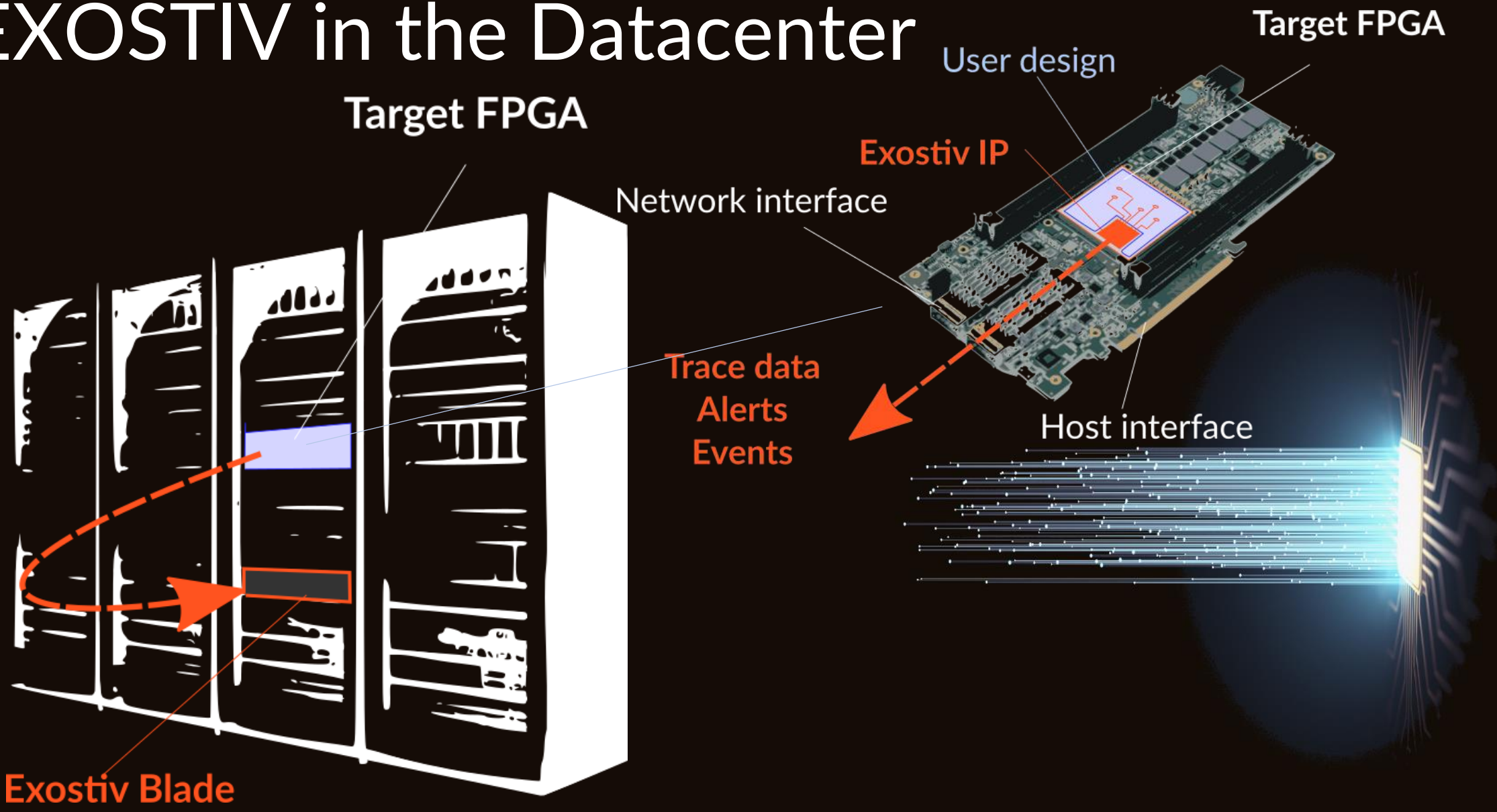
EXOSTIV LABS Visibility into the FPGA.

EXOSTIV in the lab

- 32K nodes per FPGA max
- 8 GB memory
- 50 Gbps bandwidth
- > 350 MHz operation
- Data multiplexing, triggering, filtering, event counters
- Integrated waveform viewer
- Xilinx Series 7, Ultrascale(+), Zynq / Intel Series 10 support

EXOSTIV LABS Visibility into the FPGA.

EXOSTIV in the Datacenter



EXOSTIV LABS Visibility into the FPGA.

EXOSTIV Blade

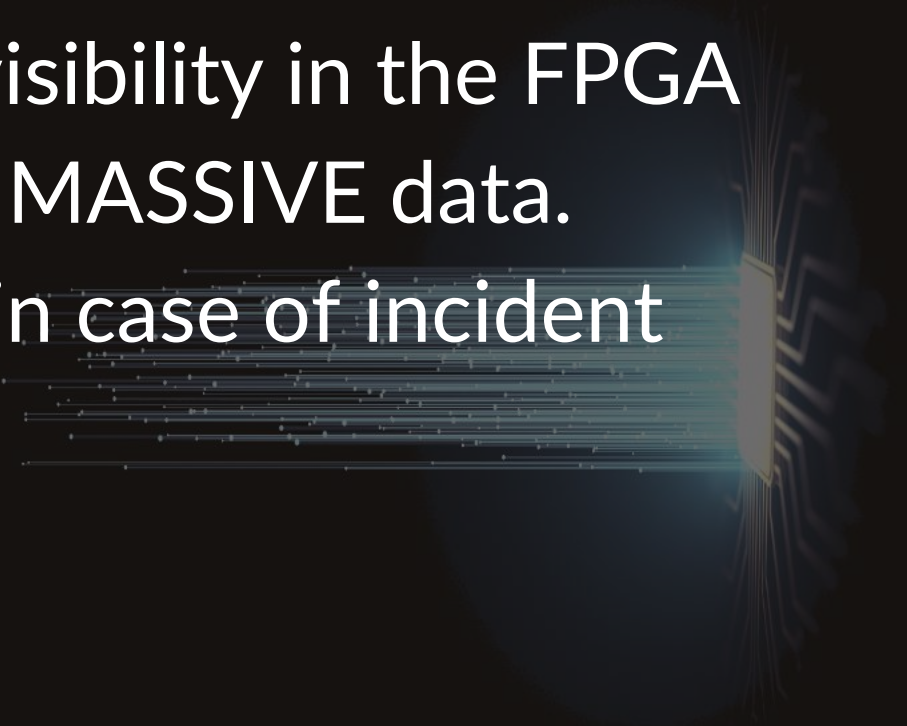
- Scale up to 1 Tbps - 80 GB memory - 10 x 100 Gbps QSFP+
- SSD local storage option or bridge to network storage

Capabilities

- Alert generation & Trace capture from inside the FPGA
  - ✓Cycle-accurate
  - ✓User-defined
  - ✓Data enrichment (timestamping, …)
  - ✓**Inside FPGA – NOT at I/O level**
- Based on finance-grade hardware
- **TERABYTES** of information with local storage.
- Scales with technology: FPGA is its own observer

Benefits

- Fine-grain FPGA algorithms control & measurements
- Visibility infrastructure available in the field & in the lab
- Extremely detailed AND extended visibility in the FPGA
- Algos assessment against REAL and MASSIVE data.
- Faster corrections turnaround time in case of incident



Thanks. Check the box for more info.