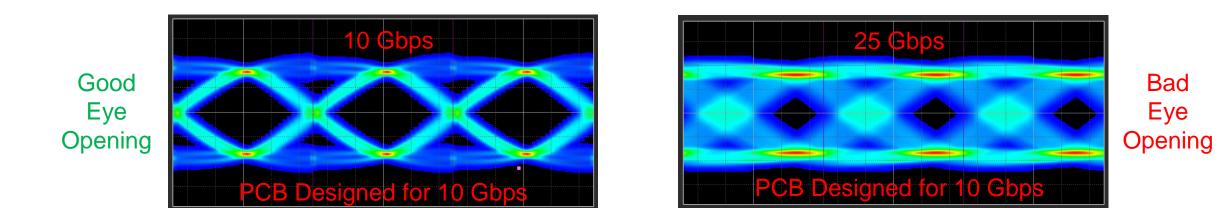
Staying Cool at Speed: Adding 25G to HFT Accelerators

STAC Summit New York Lawrence Der – Application Engineering Director May 14, 2024

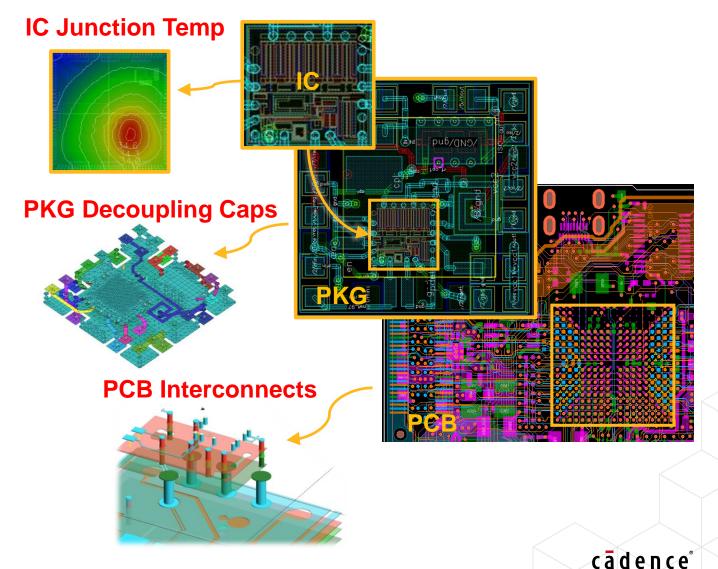
How Does 25Gbps Differ from 10Gbps?



- Signal, Power, and Thermal Integrity become much more challenging at 25Gbps
- Fast rise times and higher data rates \Rightarrow interconnects become transmission lines
- Power Distribution Network (PDN) needs to support low voltage and high current
- Increased power dissipation leads to higher junction temperatures, thermal hot spots

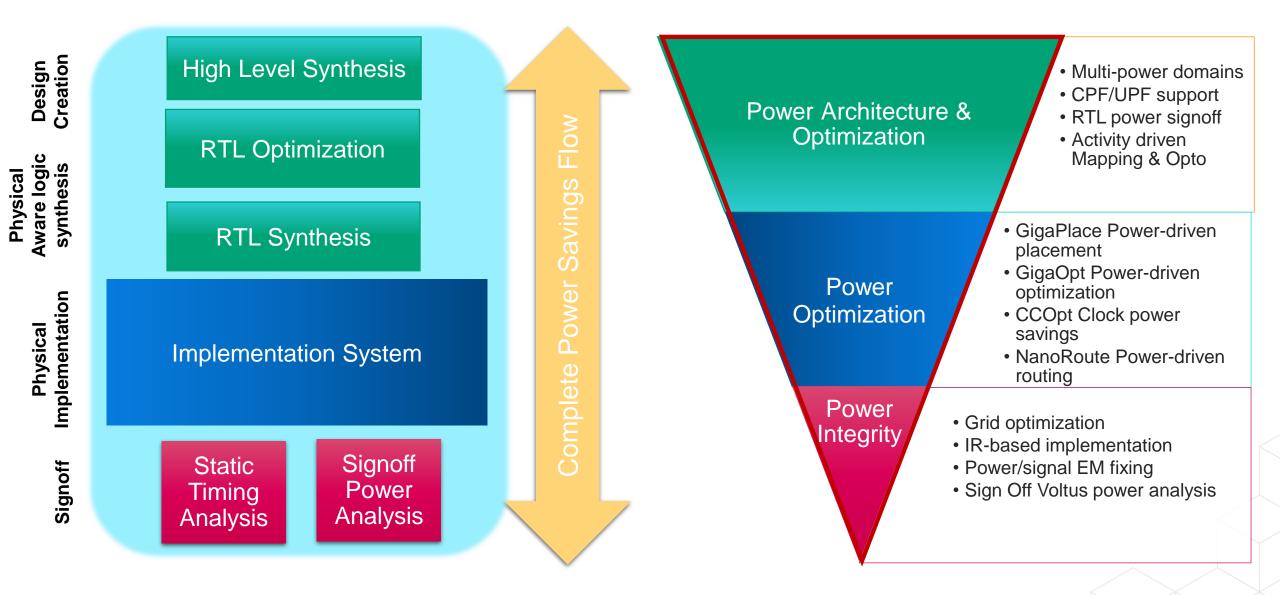
Where can Power, Thermal, and SI Issues Exists in IC, Pkg, PCB?

- At high-speeds need to consider routing at all levels: IC, PKG, PCB
- Fast data rates means higher power, increased current densities and higher temperatures
- Minimize loop inductance with decoupling capacitors at the package
- Optimize signal routes, via structures, return paths, PDN on PCB



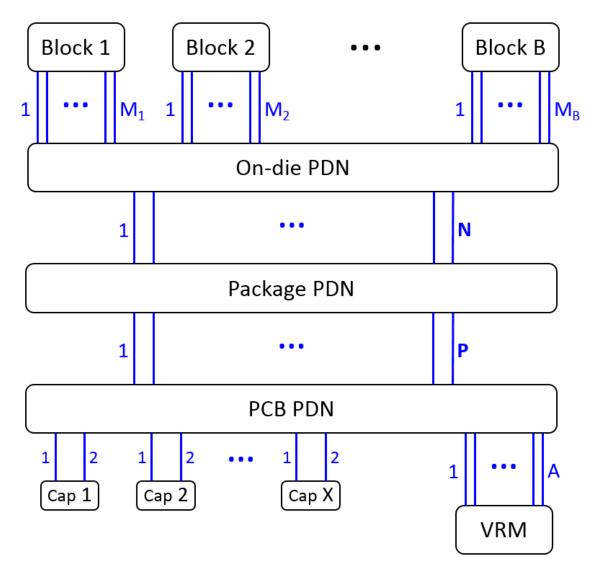
IC Power Optimization Has to Be Full Flow

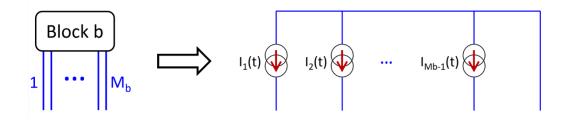
Optimize Power



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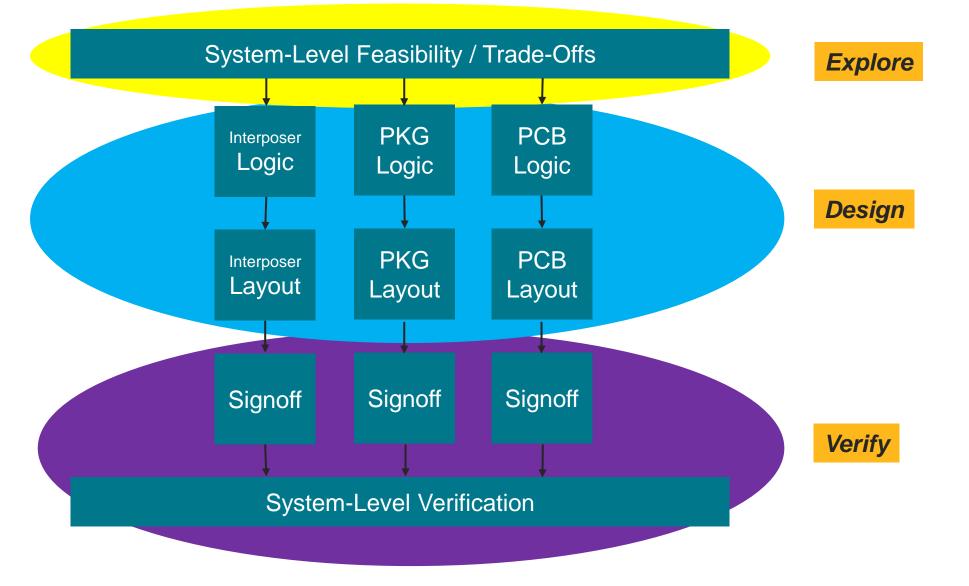
What Power Distribution Network (PDN) Does Your Chip See?



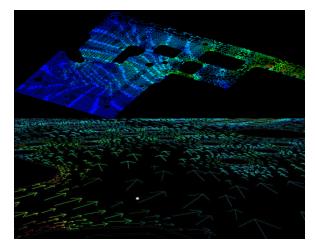


- "Clean" power comes into PCB
- Travels through multiple levels of parasitics
- Non-ideal power delivered to chip

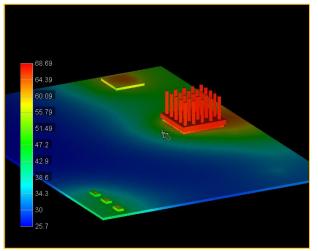
How do you address this? Multiple levels to consider ...



IR Drop and Thermal Analysis of Package / PCB



IR Drop Analysis



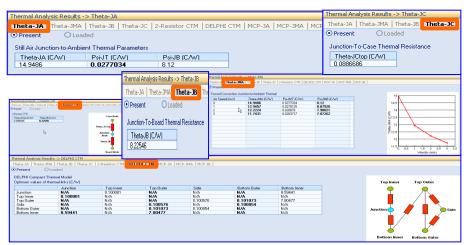
E/T Co-Simulation

Resistance Name	Model	🖶 📛 Positive Pin (GND)	-	Pin1 Name	Pin1	Pin2 Name	Pin2	Resistance (Ohn
RESI BGA1 DIE1 VDDIO	Multiple to Multiple	C 196PINBGABGA1.A1 (GND)			Net		Net	
RESI BGA1 DIE1 GND	Multiple to Multiple	Node0!!A1::GND		Node0!!A1::GND	GND	Node252711SWSIG8	GND	0.0026502
ILDI DURI DILI GIO	marapic to marapic	IB-C 196PINBGA_BGA1.A2 (GND)		Node0!!A1::GND	GND	Node2596!!SESIG3	GND	0.0026613
		B C 196PINBGA_BGA1.A3 (GND)		Node0!!A1::GND	GND	Node2458!!NWSIG3	GND	0.0026892
		 C 196PINBGA_BGA1.A4 (GND) C 196PINBGA .BGA1.A5 (GND) 	=	Node0!!A1::GND	GND	Node2389!!NESIG8	GND	0.002702
		I96PINBGA_BGA1.A5 (GND) I96PINBGA .BGA1.A6 (GND)		Node0!!A1::GND	GND	Node2525!!SWSIG8	GND	0.002746
		196PINBGABGA1.A6 (GND) 196PINBGABGA1.A7 (GND)		Node0!!A1::GND	GND	Node2521!!SWSIG7	GND	0.002759
		ISOPINEGA_BGA1.A8 (GND)		Node0!!A1::GND	GND	Node2594!!SESIG2	GND	0.002762
		(0 196711008_008_008_008_008_008_008_008_008_00		Node0!!A1::GND	GND	Node2590!!SESIG3	GND	0.002766
		196PINEGA .BGA1.A10 (GND)		Node0!!A1::GND	GND	Node2456!!NWSIG2	GND	0.002795
		0 196PINBGA .BGA1.A11 (GND)		Node0!!A1::GND	GND	Node2452!!NWSIG3	GND	0.002802
		① 196PINBGABGA1.A12 (GND)		Node0!!A1::GND	GND	Node2383!!NESIG7	GND	0.002808
		① 196PINBGABGA1.A13 (GND)		Node0!!A1::GND	GND	Node2523!!SWSIG8	GND	0.002809
				Node0!!A1::GND	GND	Node2387!!NESIG8	GND	0.002816
				Node0!!A1::GND	GND	Node2515!!SWSIG6	GND	0.002830
		B C 196PINBGA_BGA1.B2 (GND)		Node0!!A1::GND	GND	Node2584!!SESIG3	GND	0.00283
		I96PINBGA_BGA1.B3 (GND)		Node0!!A1::GND	GND	Node2592!!SESIG1	GND	0.002834
		International Control (International International Inte		Node0!!A1::GND	GND	Node2532!!SWSIG8	GND	0.002848
		III C 196PINBGABGA1.B9 (GND)		Node0!!A1::GND	GND	Node2579!!SESIG3	GND	0.002862
		B C 196PINBGA_BGA1.B10 (GND)		Node0!!A1::GND	GND	Node2510!!SWSIG5	GND	0.002875
		B C 196PINBGABGA1.B11 (GND)		Node0!!A1::GND	GND	Node2454!!NWSIG1	GND	0.002876
		B-C 196PINBGA_BGA1.B12 (GND)		Node0!!A1::GND	GND	Node2538!!SWSIG8	GND	0.002877
		196PINBGA_BGA1.B13 (GND) 196PINBGA .BGA1.B14 (GND)		Node0!!A1::GND	GND	Node2601!!SESIG8	GND	0.002881
				Node0!!A1::GND	GND	Node2377!!NESIG6	GND	0.00288
		B (C) 196PINBGA_BGA1.C1 (GND)		Node0!!A1::GND	GND	Node2574!!SESIG3	GND	0.002884
		(C) 196PINBGA_BGA1.C12 (GND) (C) 196PINBGA _BGA1.C13 (GND)		Node0!!A1::GND	GND	Node2446!!NWSIG3	CND	0.002892

Resistance Ana	lysis Setup -> Se	t up Eq. Resistance Ne	twork				
Add Terminal	Delete Terminal	Change Output File	🗹 Us	e File Name Pattern	Short VRM	Other Circuit	
Output File Nan	ne: D:\Cadence\S	igrity2019\share\Speed	XP\San	nples\PowerDC\Electr	ical Analysis\Spicel	Netlist.ckt	
Terminal Name						GND -1.4000000000	0000 -0.600000000000
DIE1.NESIG1	001			*SWSIG5003	DIE1_SWSIG5003	GND -1.4000000000	0000 -0.80000000000
DIE 1.NESIG 10	003		=				0000 -1.00000000000000000000000000000000
DIE1.NESIG2	001		-	*SWSIG8001	DIE1_SWSIG8001	GND -1.0000000000	0000 -1.40000000000
DIE1.NESIG2							0000 -1.40000000000
DIE1.NESIG3				*SWSIG8004	DIE1 SWSIG8004	GND -0.8000000000	0000 -1.400000000000
DIE 1.NESIG3							0000 -1.40000000000
DIE1.NESIG4							0000 -1.4000000000000000000000000000000000000
DIE1.NESIG4							
				* IMCP Endl			
DIE1.NESIG5				*			
DIE1.NESIG5				*This concl	Ludes the MCP se	ction	
DIE1.NESIG6				RO DIEL NES	SIG2001 DIE1 NES	IG1001 0.02092590843	75
DIE1.NESIG6				R1 DIE1 NES	SIG3001 DIEL NES	IG2001 0.02100891771	44
DIE1.NESIG6	004					IG2001 0.03648267260 IG2001 0.06582783381	
DIE1.NESIG6	005			R4 DIE1 NES	SIG6001 DIEL NES	IG2001 0.14577420135	2
DIE1.NESIG6	006					IG2001 0.13920346908 IG2001 0.23044797049	
DIE 1.NESIG6	007					IG2001 0.35690896467	
DIE1.NESIG7	003					IG2001 0.52929414998	
DIE1.NESIG8	001					IG2001 0.76604140424 SIG2001 1.0886200365	
DIE1.NESIG8	002			R11 DIEL N	SIG1003 DIE1 NE	SIG2001 1.5314866824	4
DIE 1.NESIG8	003					SIG2001 2.1470347411 SIG2001 3.2509353693	
DIE1.NESIG8	004			R14 DIEL N	SIG1006 DIE1 NE	SIG2001 6.8871506314	3
DIE1.NESIG8						SIG2001 6.0246314584	
DIE1.NESIG8						SIG2001 9.2343163664 SIG2001 13.103080432	
DIE1.NESIGO						SIG2001 17.126766722	

DIE1.NESIG8007

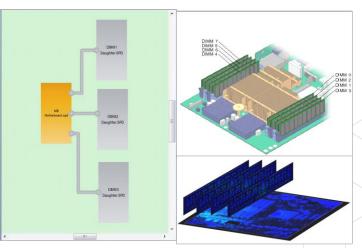
Resistance Measurement



Thermal Model Extraction

Resistance Network Generation

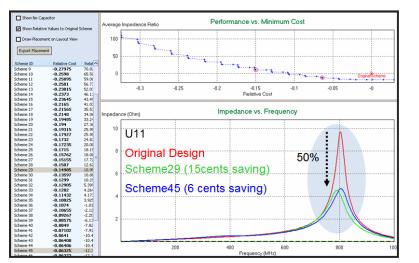
R19 DIE1 SESIF1004 DIE1 NESIG2001 0.48181232888



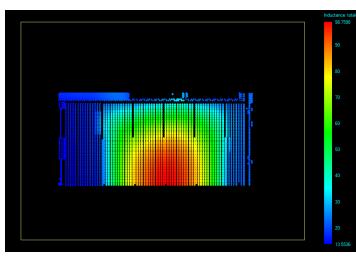
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Multi-Board Analysis

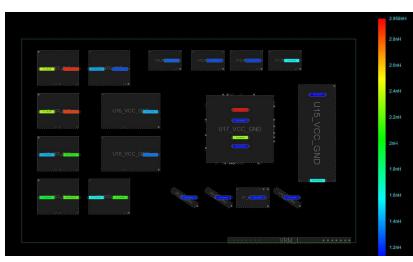
AC Analysis of Package / PCB



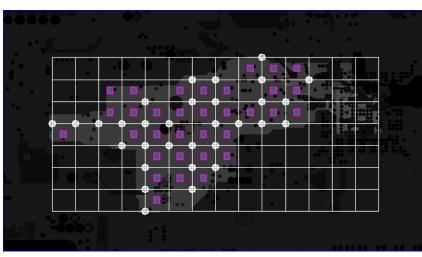
Pre- and Post-Layout Optimization



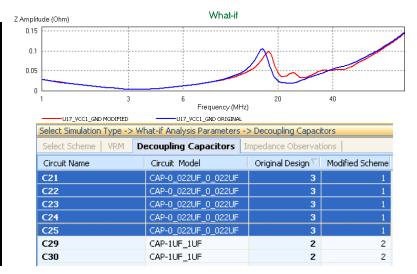
IC Device Power Pin Inductance



Decoupling Capacitor Loop Inductance



EMI Capacitor Optimization



What-if Analysis



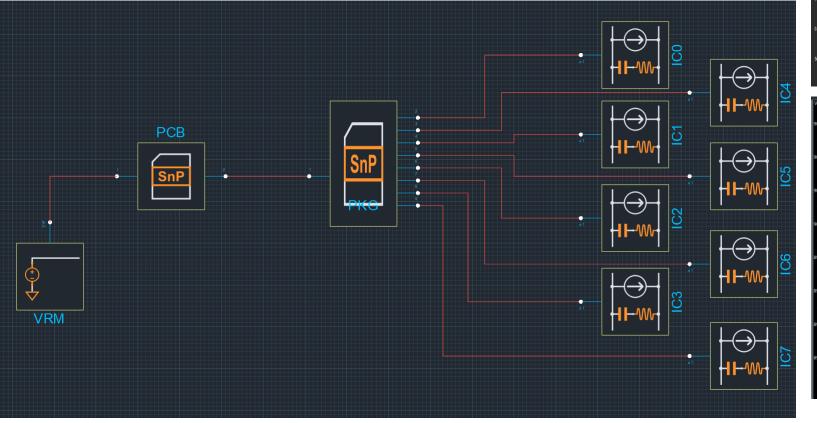
PDN Impedance Check

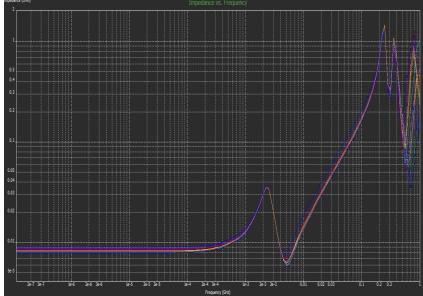
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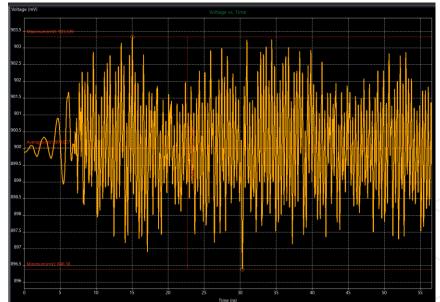
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System-Level PI Analysis

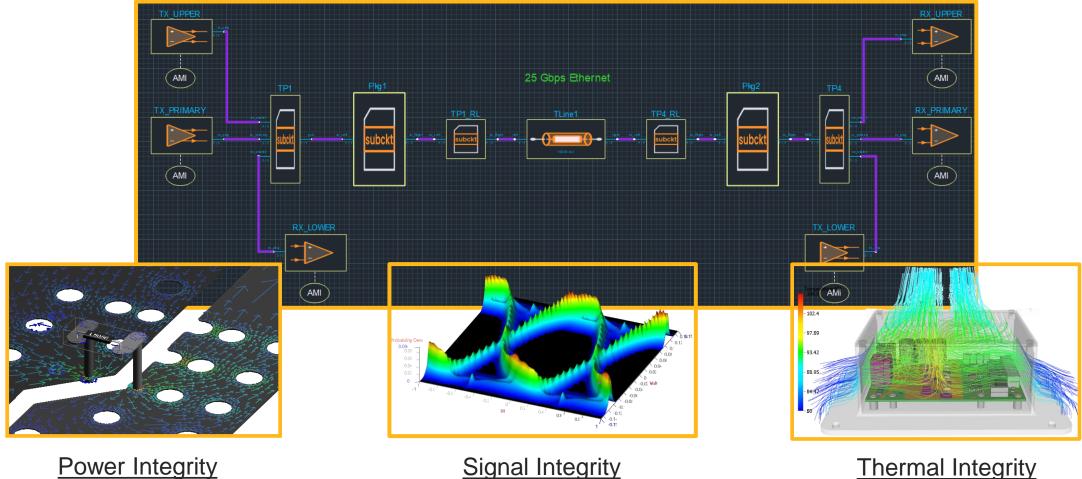
- Put packages and PCB(s) all together for complete PDN
- Check frequency domain vs. target impedance
- Check time domain vs. ripple spec







Cadence MSA Technology Enables High-Speed Operation



Operate at low supply voltages Eliminate high current density spots Meet PDN AC impedance

Signal Integrity

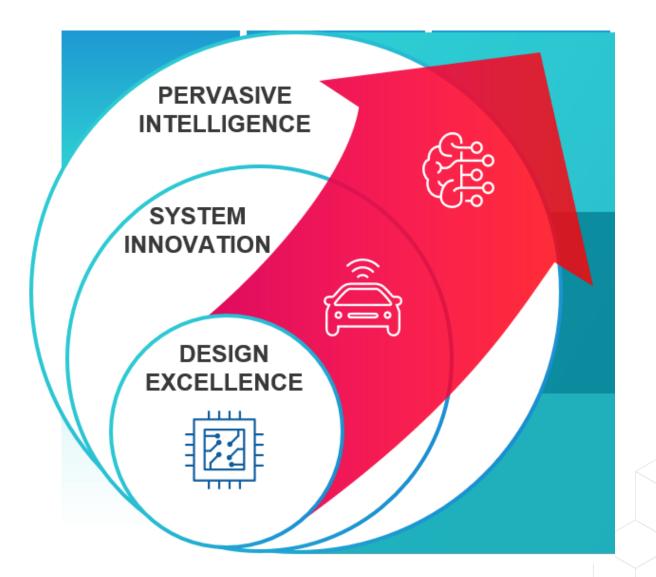
Optimized Signal/Return-path routing Minimize reflections and crosstalk Validate System Compliance

Thermal Integrity

Guarantee Junction Temperatures Eliminate thermal hot spots Optimize system cooling cādence

Staying Cool Summary

- Signal, Power, and Thermal Integrity become much more challenging at high-speeds
- Fast data rates means higher power consumption, increased current densities, and higher temperatures must be considered in the design process
- High-speed signal routes, via structures, return paths must be designed with transmission lines and modeled with electromagnetic extractions
- The complexity of high-performance systems design is an iterative, resource intensive, and expensive process that can benefit from AI driven analysis
- Cadence offers the complete solution of design platforms, multi-physics analysis engines, and is now bringing AI to bear on the system design problem



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