Staying Cool at Speed: Adding 25G to HFT Accelerators

STAC Summit New York

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May 14, 2024

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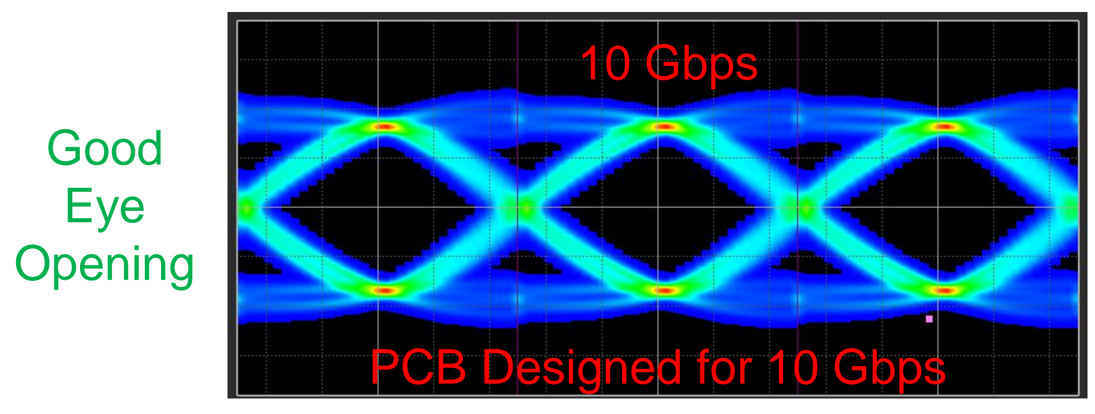
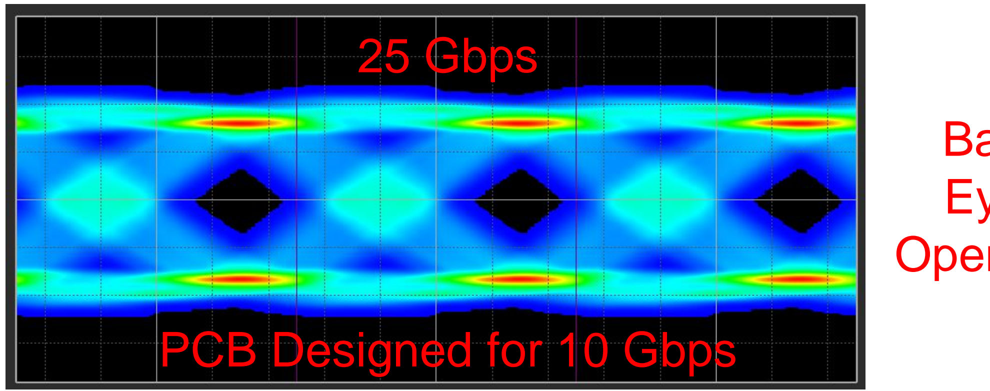
How Does 25Gbps Differ from 10Gbps?

Good Eye Opening





Bad Eye Opening

- Signal, Power, and Thermal Integrity become much more challenging at 25Gbps
- Fast rise times and higher data rates $\Rightarrow$ interconnects become transmission lines
- Power Distribution Network (PDN) needs to support low voltage and high current
- Increased power dissipation leads to higher junction temperatures, thermal hot spots

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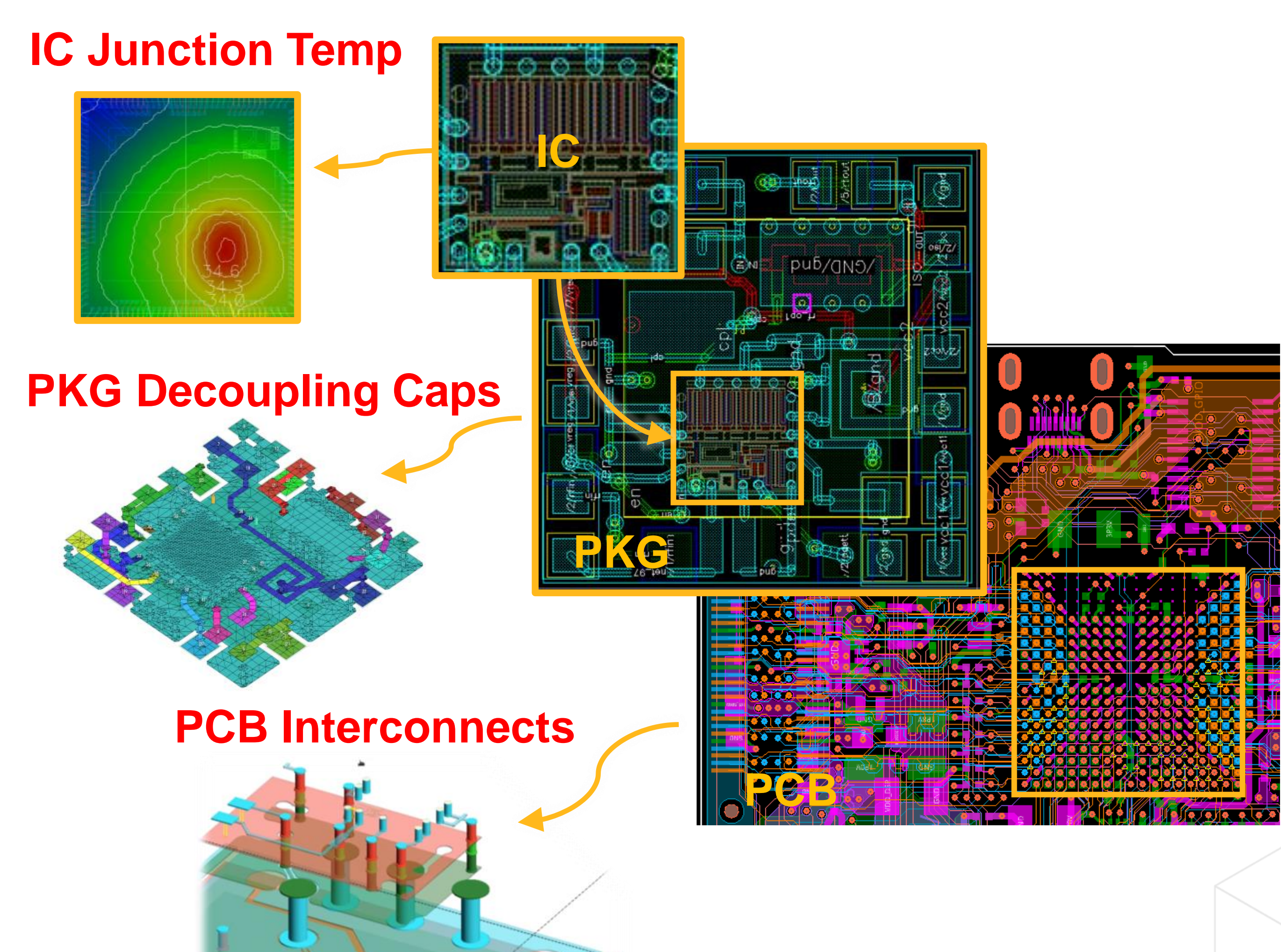
Where can Power, Thermal, and SI Issues Exists in IC, Pkg, PCB?

- At high-speeds need to consider routing at all levels: IC, PKG, PCB
- Fast data rates means higher power, increased current densities and higher temperatures
- Minimize loop inductance with decoupling capacitors at the package
- Optimize signal routes, via structures, return paths, PDN on PCB



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IC Power Optimization Has to Be Full Flow

Optimize Power

Design Creation
Physical Aware logic synthesis
Physical Implementation
Signoff

High Level Synthesis

RTL Optimization

RTL Synthesis

Implementation System

Static Timing Analysis

Signoff Power Analysis

Complete Power Savings Flow

Power Architecture & Optimization

- Multi-power domains
- CPF/UPF support
- RTL power signoff
- Activity driven Mapping & Opto

Power Optimization

- GigaPlace Power-driven placement
- GigaOpt Power-driven optimization
- CCOpt Clock power savings
- NanoRoute Power-driven routing

Power Integrity

- Grid optimization
- IR-based implementation
- Power/signal EM fixing
- Sign Off Voltus power analysis

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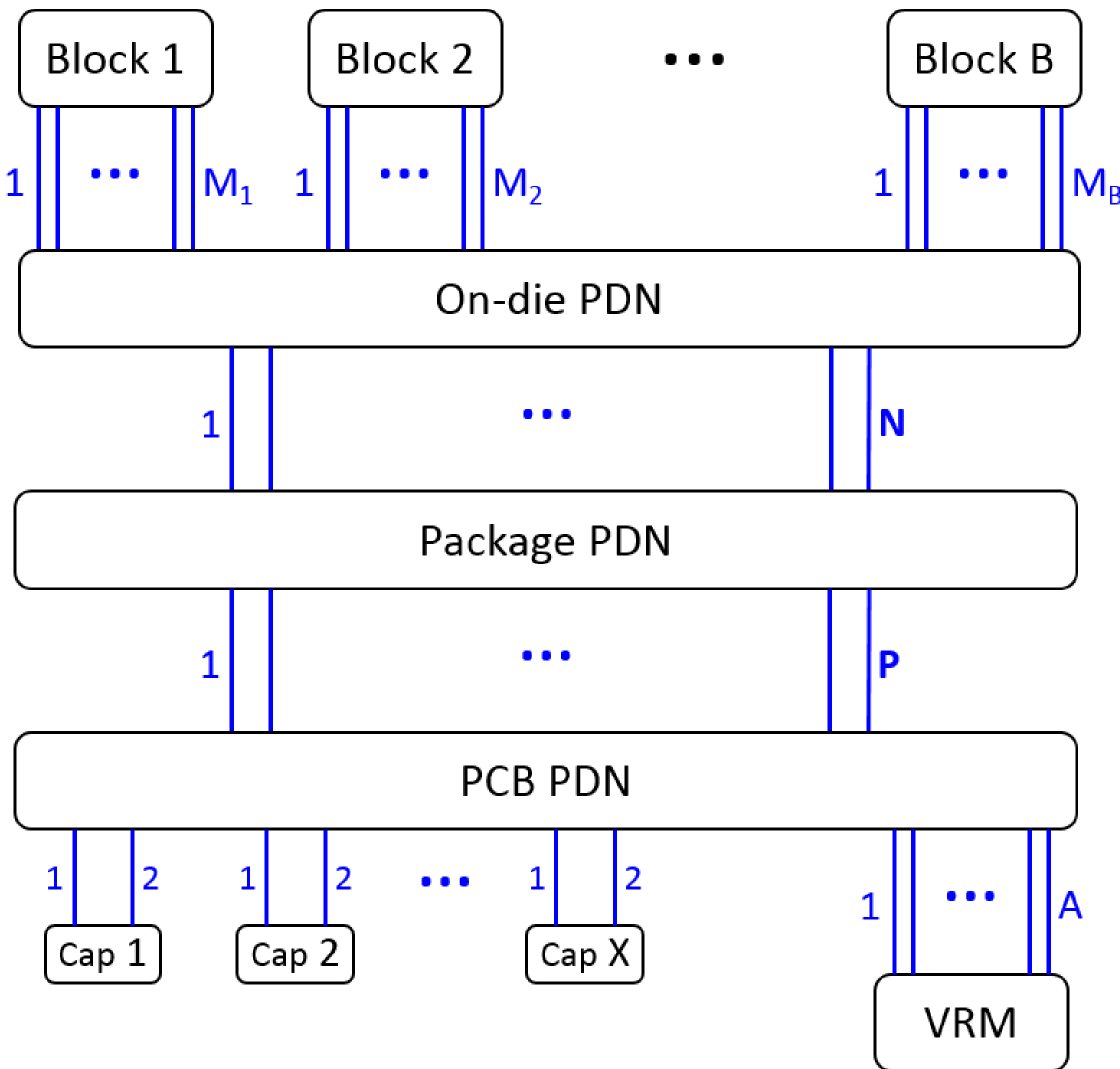
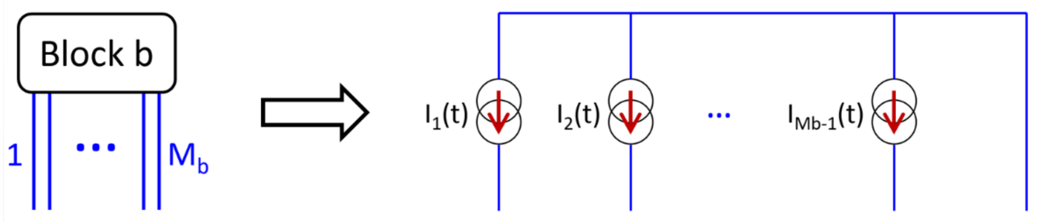
What Power Distribution Network (PDN) Does Your Chip See?





- “Clean” power comes into PCB
- Travels through multiple levels of parasitics
- Non-ideal power delivered to chip

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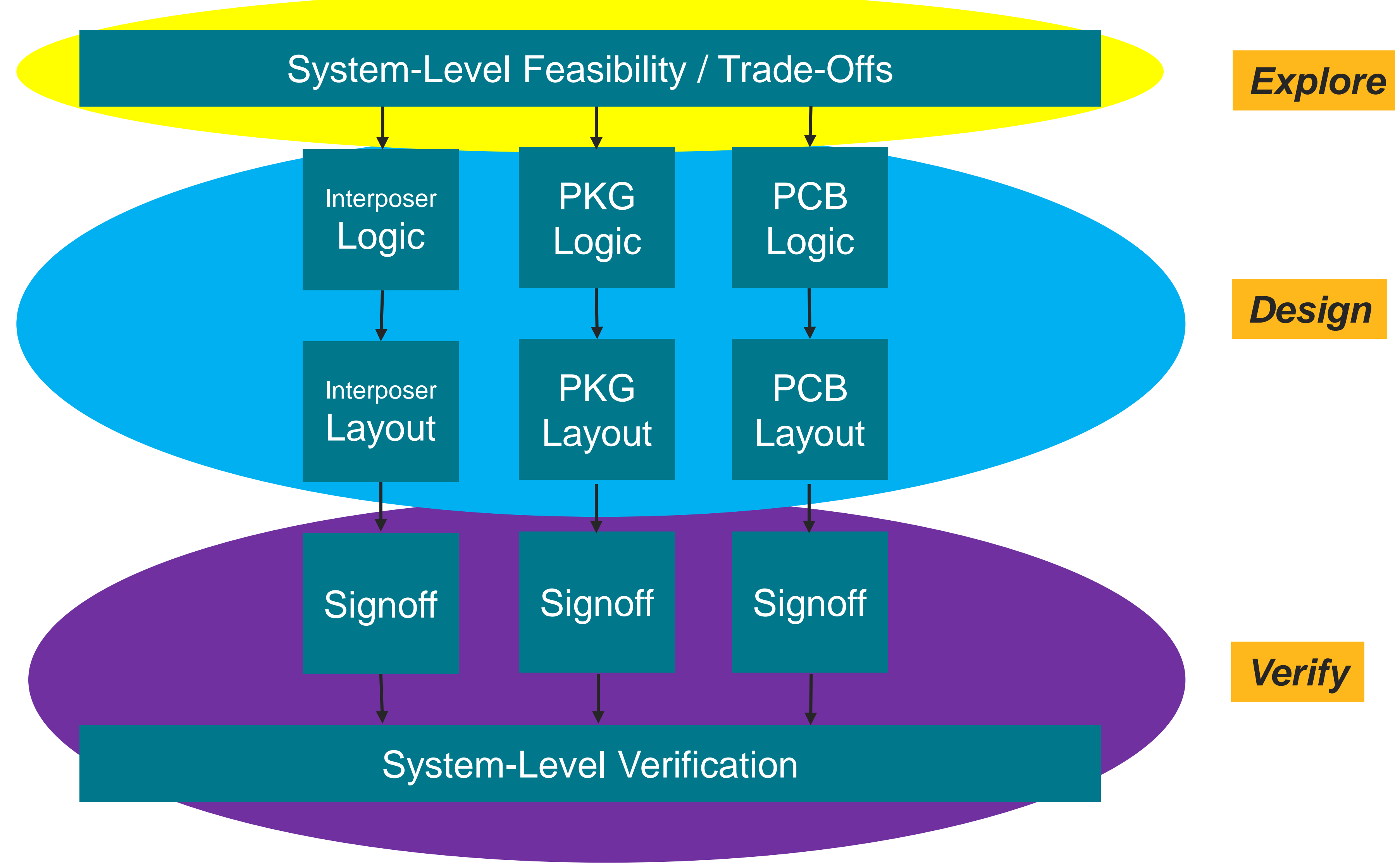
How do you address this? Multiple levels to consider …



Explore

Design

Verify

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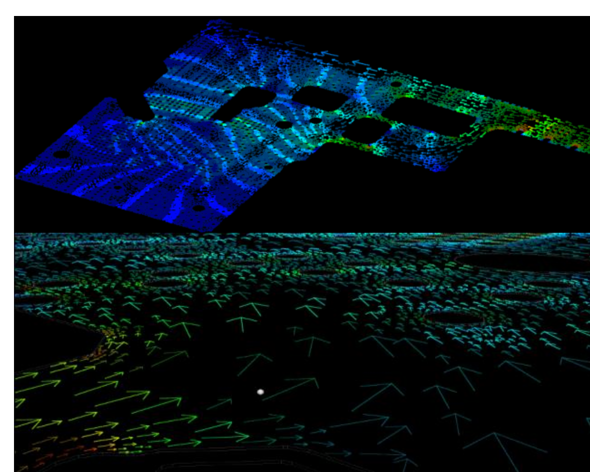
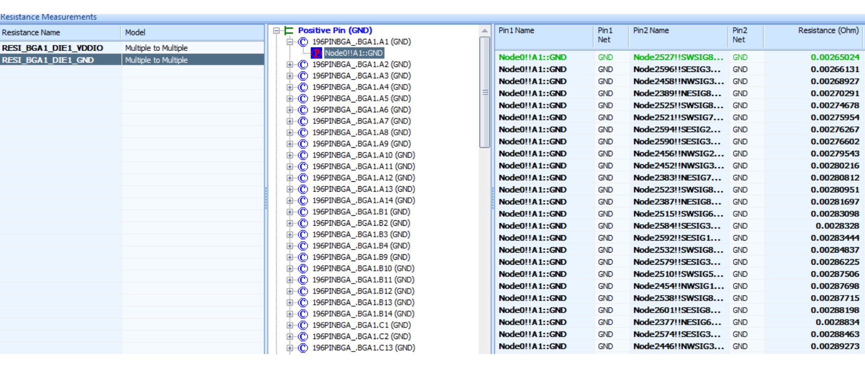
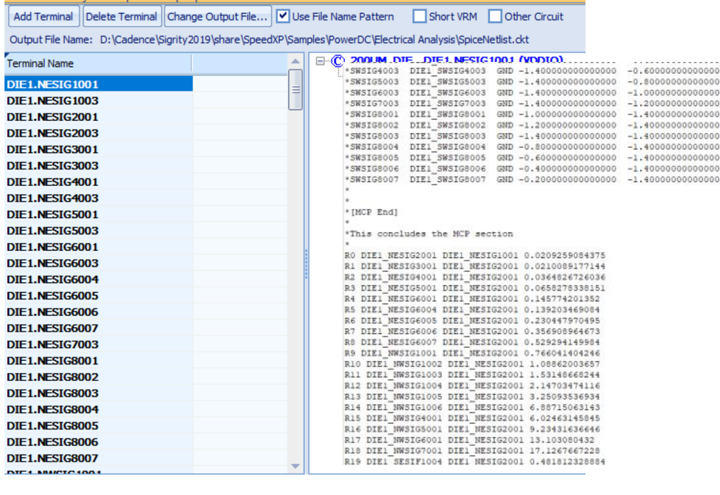
IR Drop and Thermal Analysis of Package / PCB



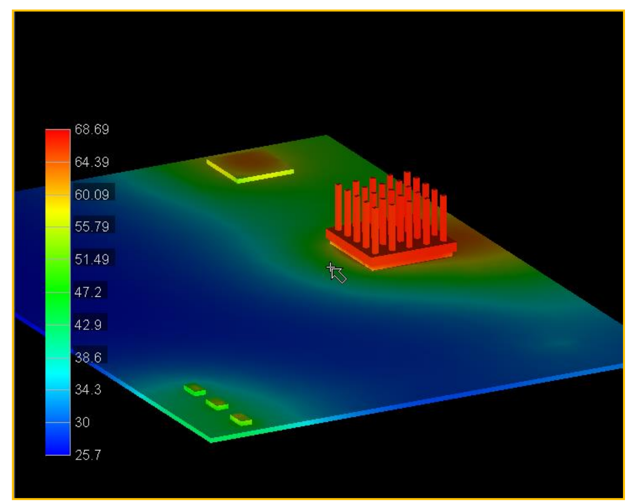
IR Drop Analysis



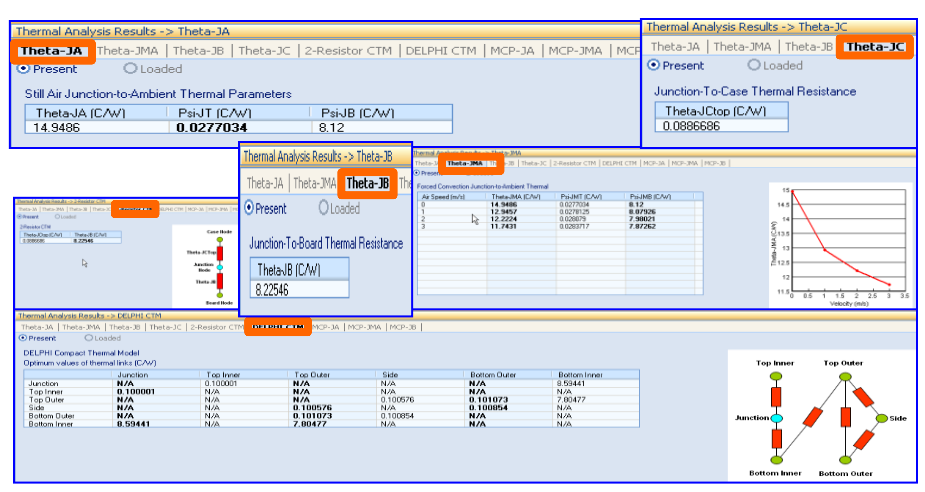
Resistance Measurement



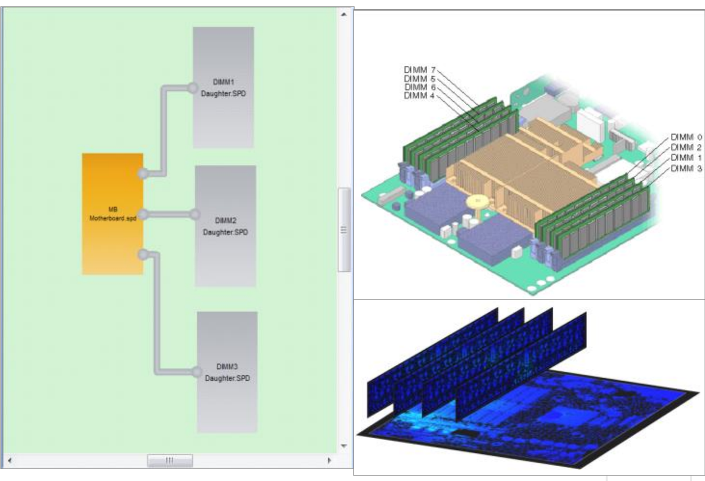
Resistance Network Generation



E/T Co-Simulation



Thermal Model Extraction



Multi-Board Analysis

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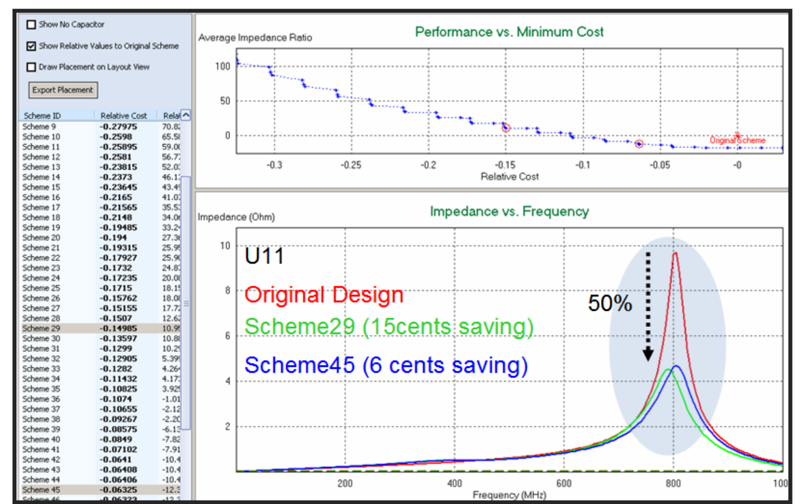
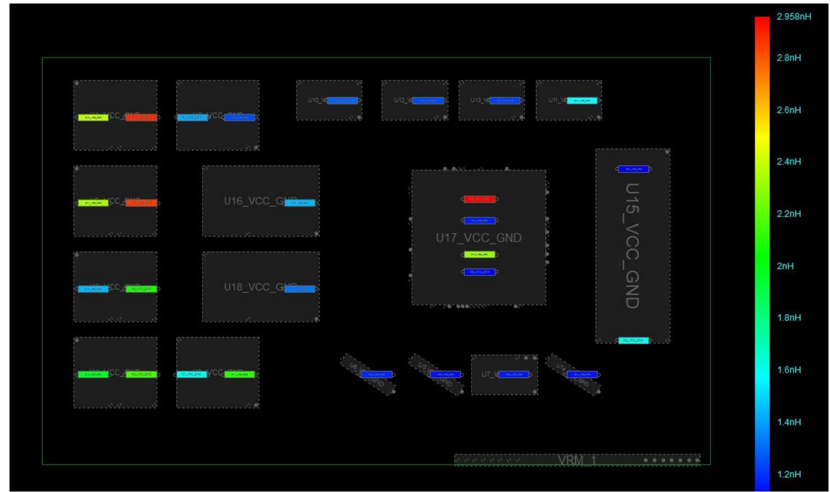
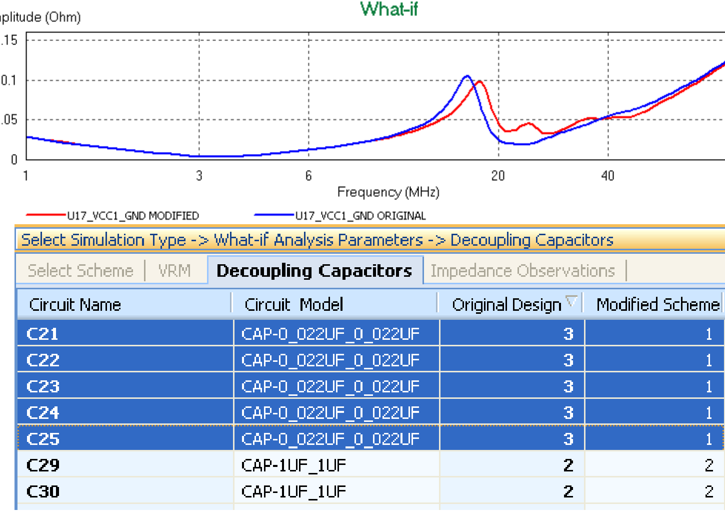
AC Analysis of Package / PCB



Pre- and Post-Layout Optimization

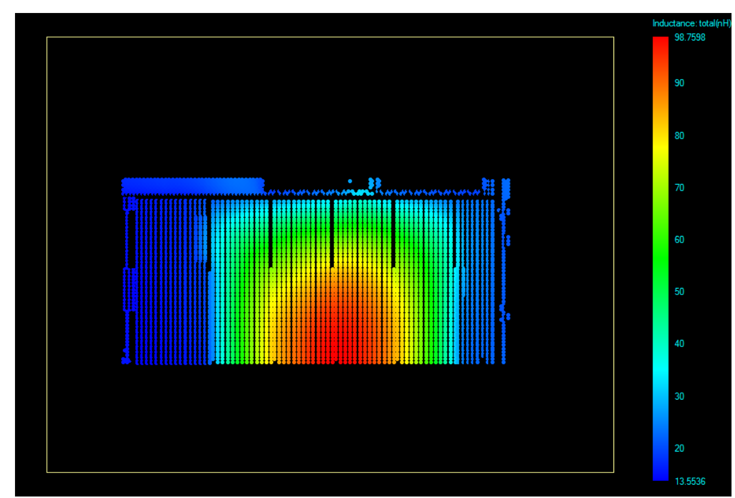


Decoupling Capacitor Loop Inductance

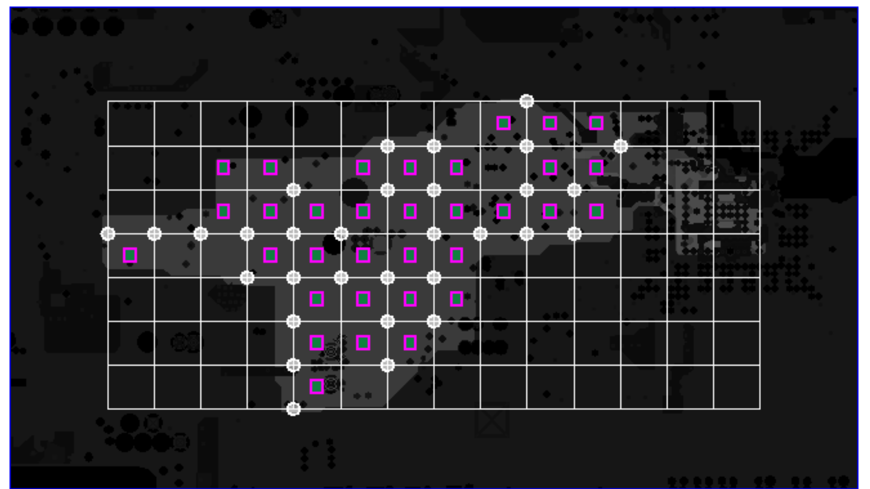


Circuit Name	Circuit Model	Original Design	Modified Scheme
C21	CAP-0_022UF_0_022UF	3	1
C22	CAP-0_022UF_0_022UF	3	1
C23	CAP-0_022UF_0_022UF	3	1
C24	CAP-0_022UF_0_022UF	3	1
C25	CAP-0_022UF_0_022UF	3	1
C29	CAP-1UF_1UF	2	2
C30	CAP-1UF_1UF	2	2

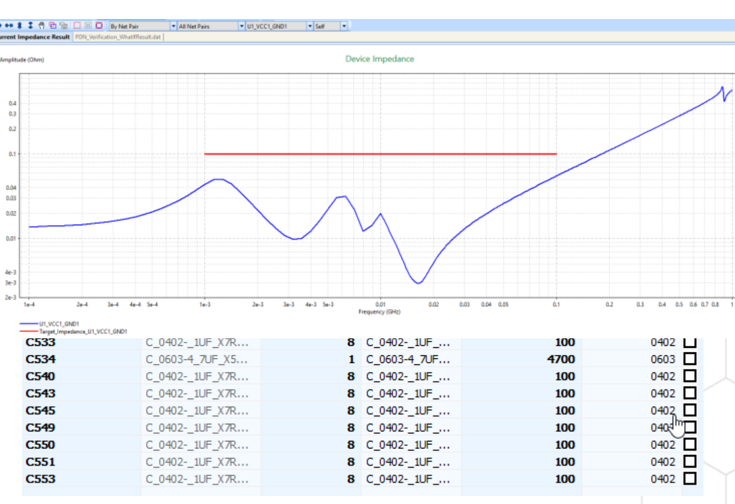
What-if Analysis



IC Device Power Pin Inductance



EMI Capacitor Optimization



PDN Impedance Check

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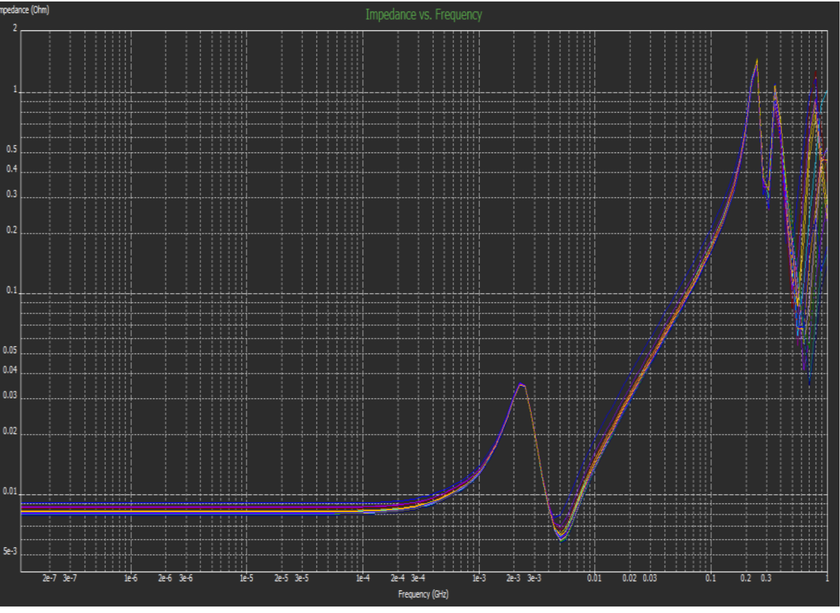
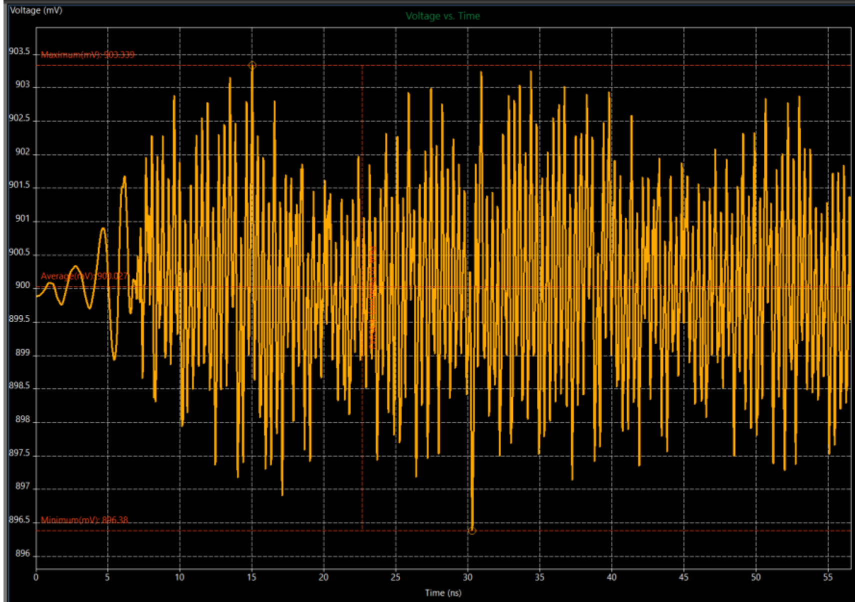
System-Level PI Analysis

- Put packages and PCB(s) all together for complete PDN
- Check frequency domain vs. target impedance
- Check time domain vs. ripple spec





PCB
SnP
PKG
VRM
IC0
IC1
IC2
IC3
IC4
IC5
IC6
IC7

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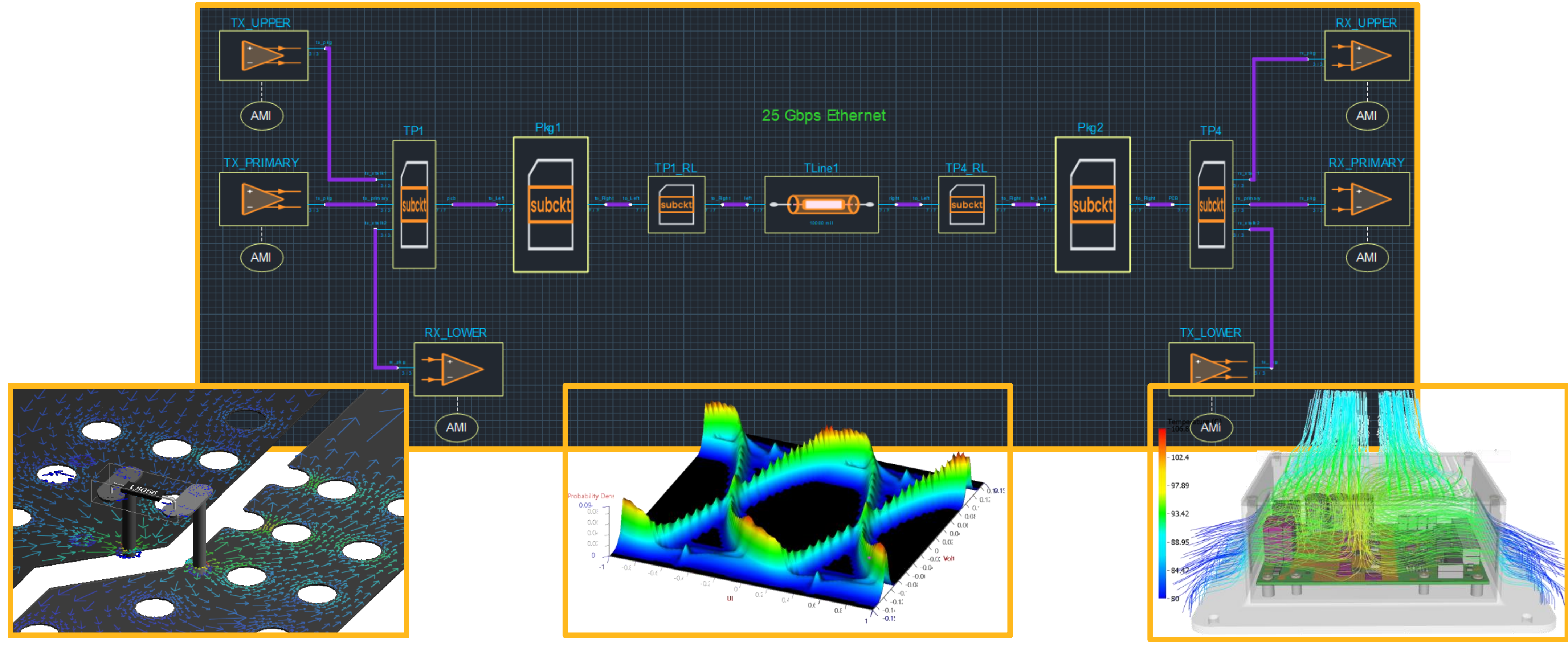
Cadence MSA Technology Enables High-Speed Operation



<u>Power Integrity</u>

Operate at low supply voltages
Eliminate high current density spots
Meet PDN AC impedance

<u>Signal Integrity</u>

Optimized Signal/Return-path routing
Minimize reflections and crosstalk
Validate System Compliance

<u>Thermal Integrity</u>

Guarantee Junction Temperatures
Eliminate thermal hot spots
Optimize system cooling

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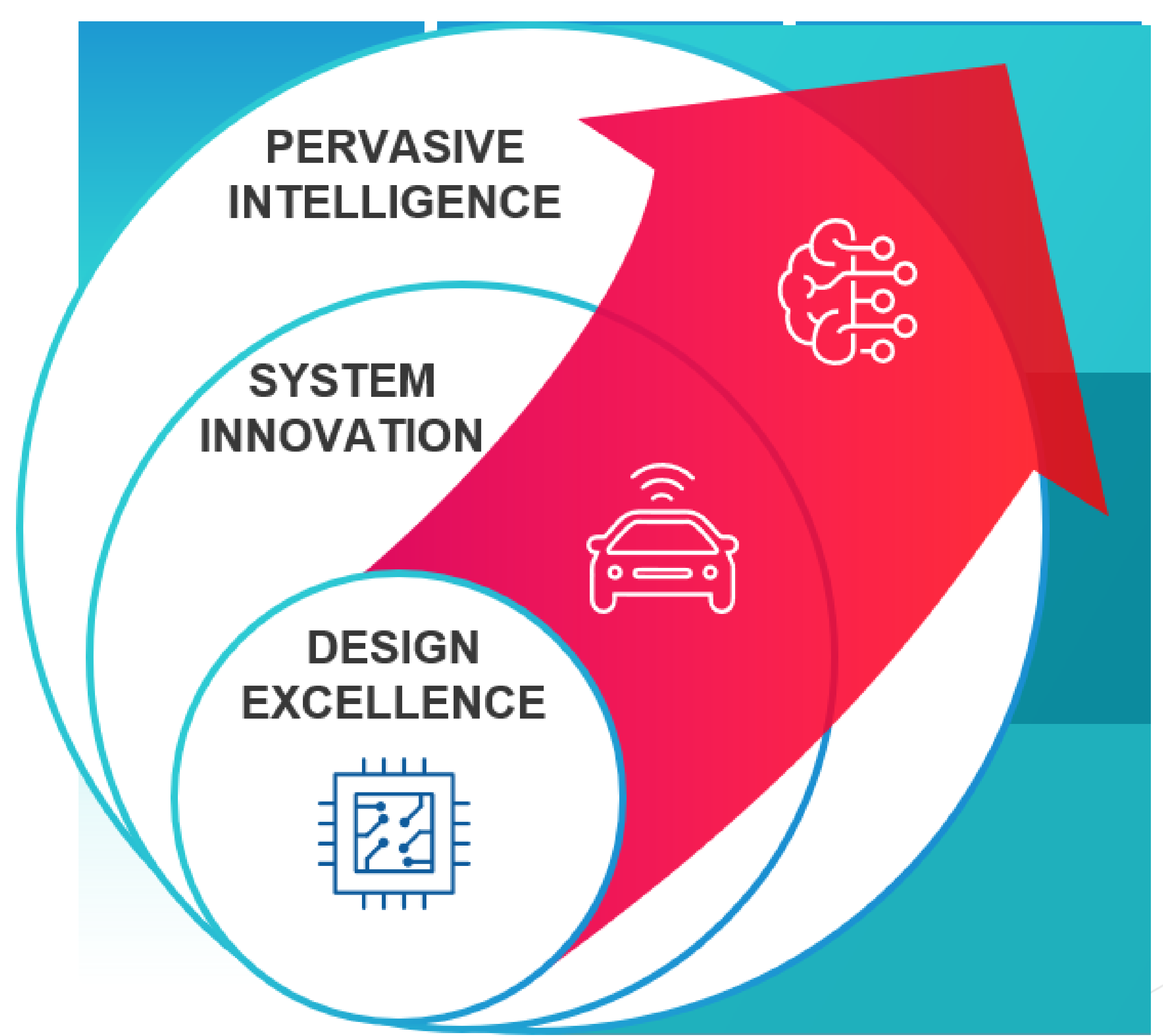
Staying Cool Summary

- Signal, Power, and Thermal Integrity become much more challenging at high-speeds
- Fast data rates means higher power consumption, increased current densities, and higher temperatures must be considered in the design process
- High-speed signal routes, via structures, return paths must be designed with transmission lines and modeled with electromagnetic extractions
- The complexity of high-performance systems design is an iterative, resource intensive, and expensive process that can benefit from AI driven analysis
- Cadence offers the complete solution of design platforms, multi-physics analysis engines, and is now bringing AI to bear on the system design problem



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