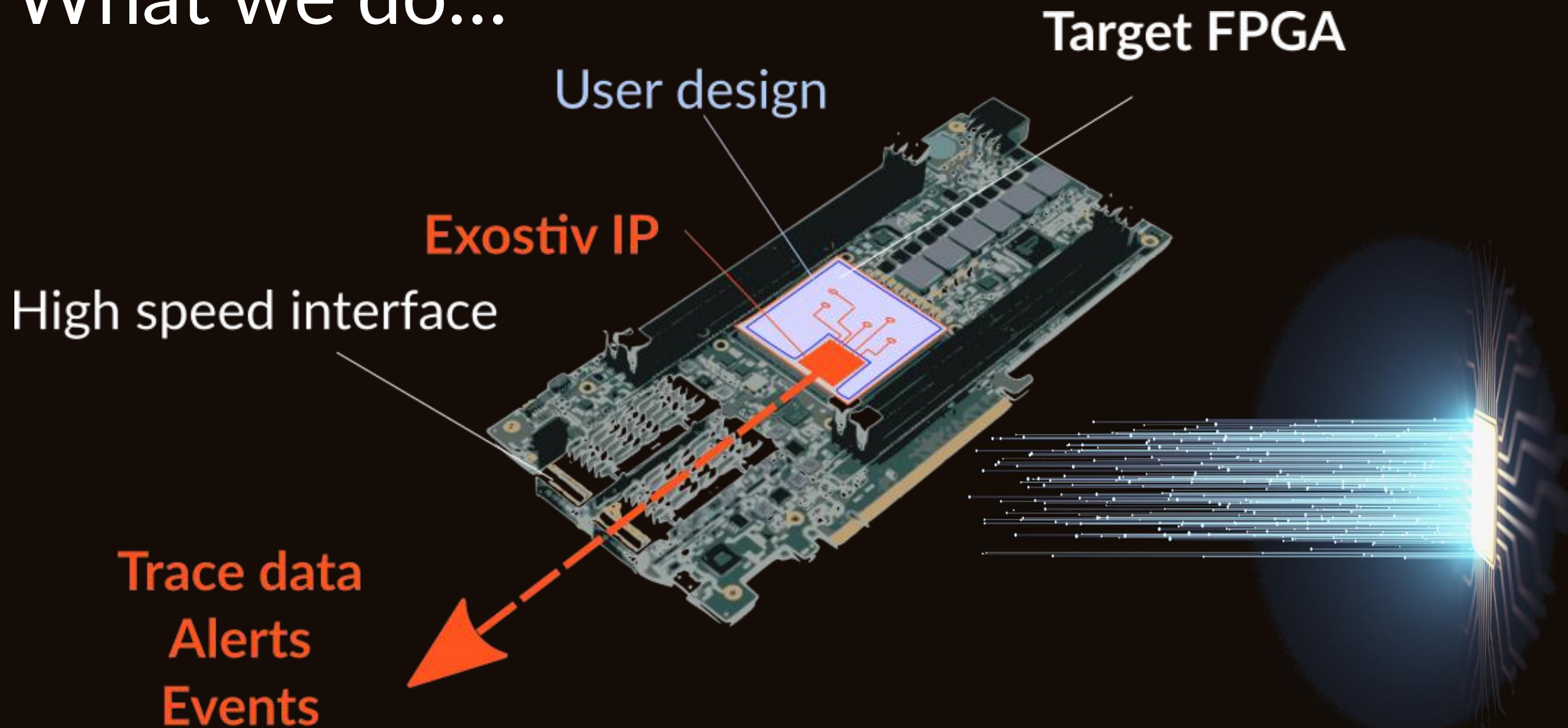


Do you *really* know what happens inside your FPGA?



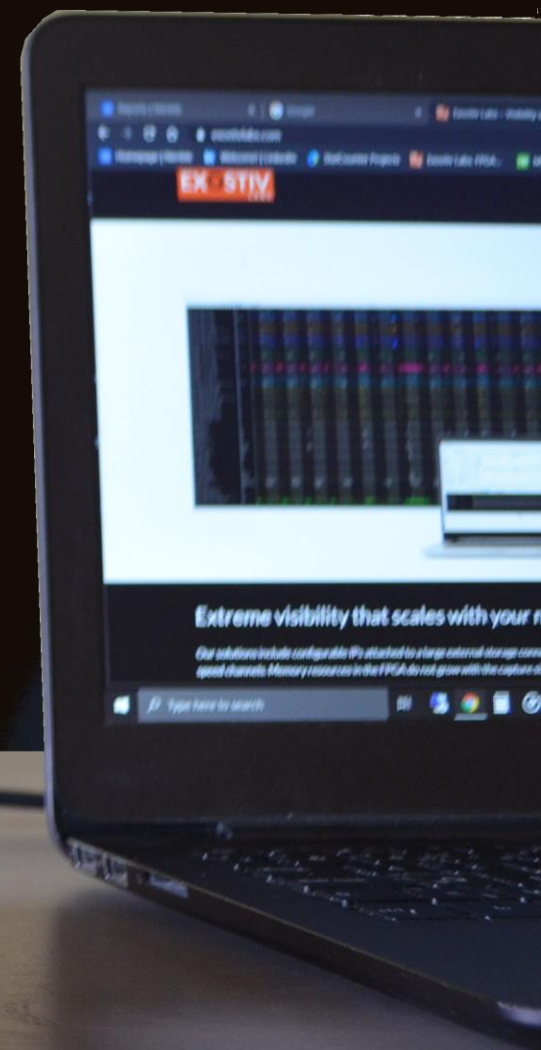
What we do...



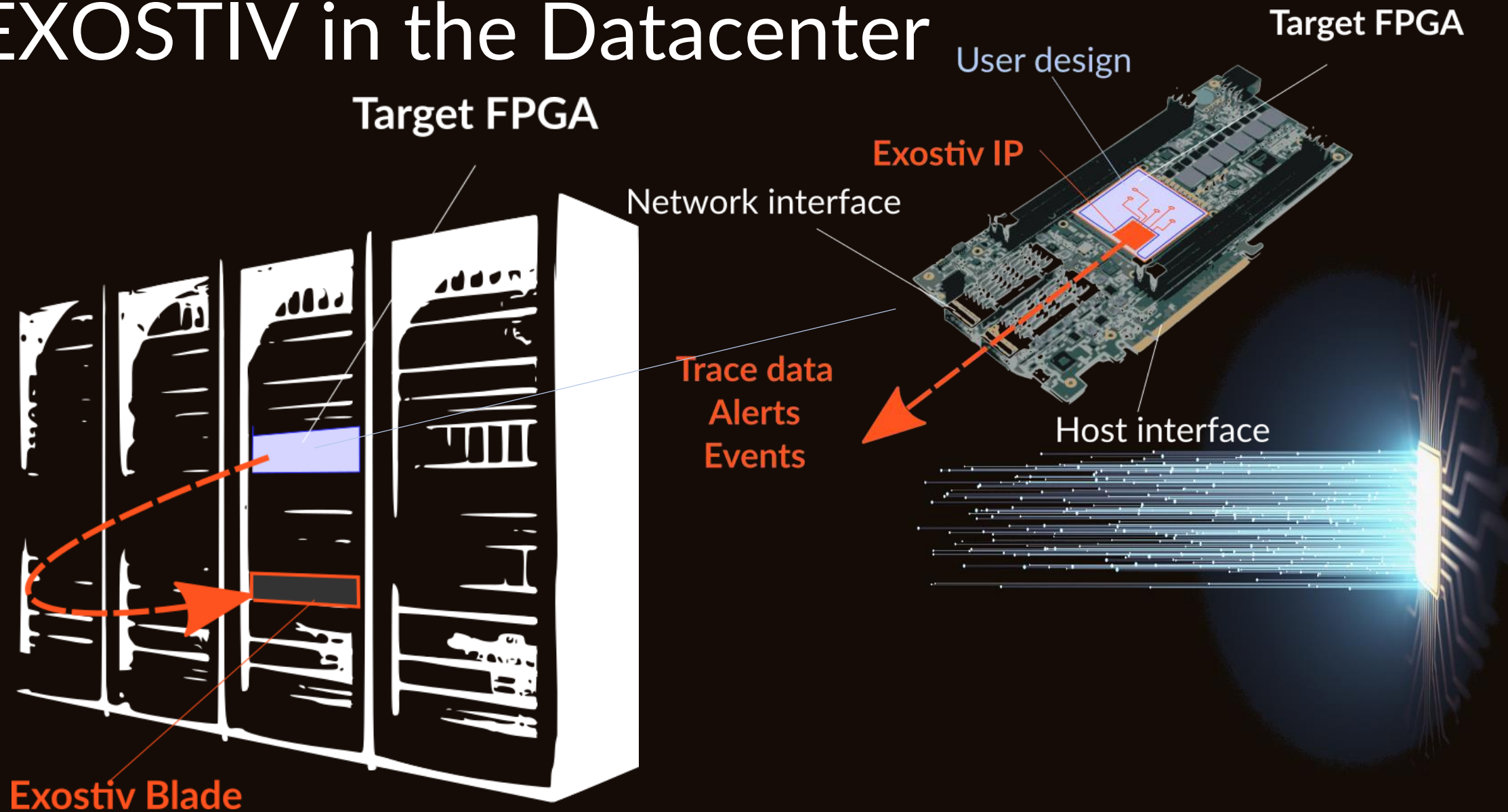


EXOSTIV in the lab

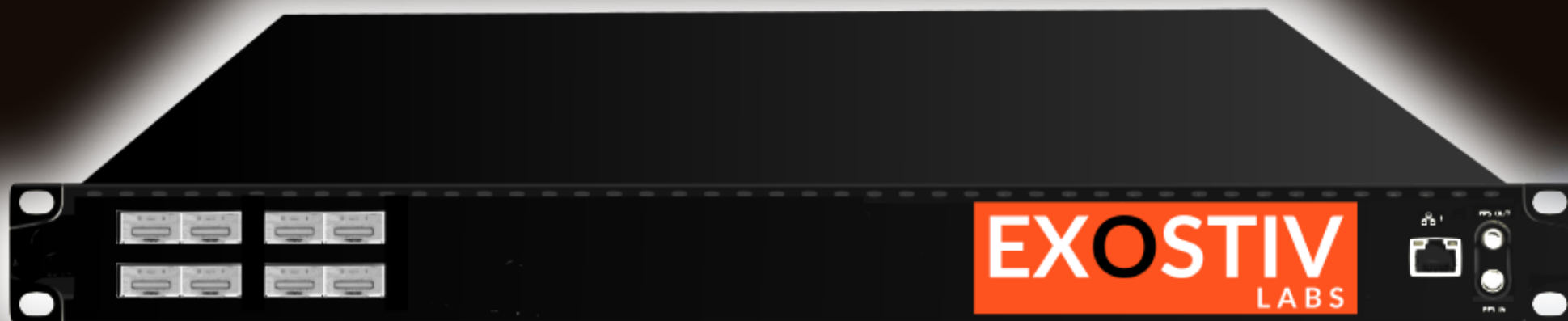
- 32K nodes per FPGA max
- 8 GB memory
- 50 Gbps bandwidth
- > 350 MHz operation
- Data multiplexing, triggering, filtering, event counters
- Integrated waveform viewer
- Xilinx Series 7, Ultrascale(+), Zynq / Intel Series 10 support



EXOSTIV in the Datacenter



EXOSTIV Blade



- Scale up to 1 Tbps - 80 GB memory - 10 x 100 Gbps QSFP+
- SSD local storage option or bridge to network storage



Capabilities

- Alert generation & Trace capture from inside the FPGA
 - ✓ Cycle-accurate
 - ✓ User-defined
 - ✓ Data enrichment (timestamping, ...)
 - ✓ **Inside FPGA – NOT at I/O level**
- Based on finance-grade hardware
- **TERABYTES** of information with local storage.
- Scales with technology: FPGA is its own observer



Benefits

- Fine-grain FPGA algorithms control & measurements
- Visibility infrastructure available in the field & in the lab
- Extremely detailed AND extended visibility in the FPGA
- Algos assessment against REAL and MASSIVE data.
- Faster corrections turnaround time in case of incident



Thanks. Check the box for more info.

