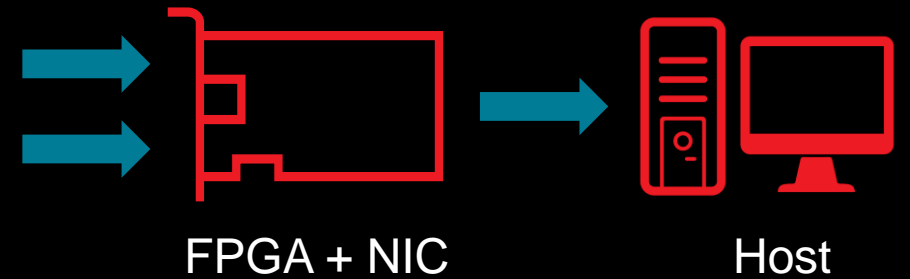




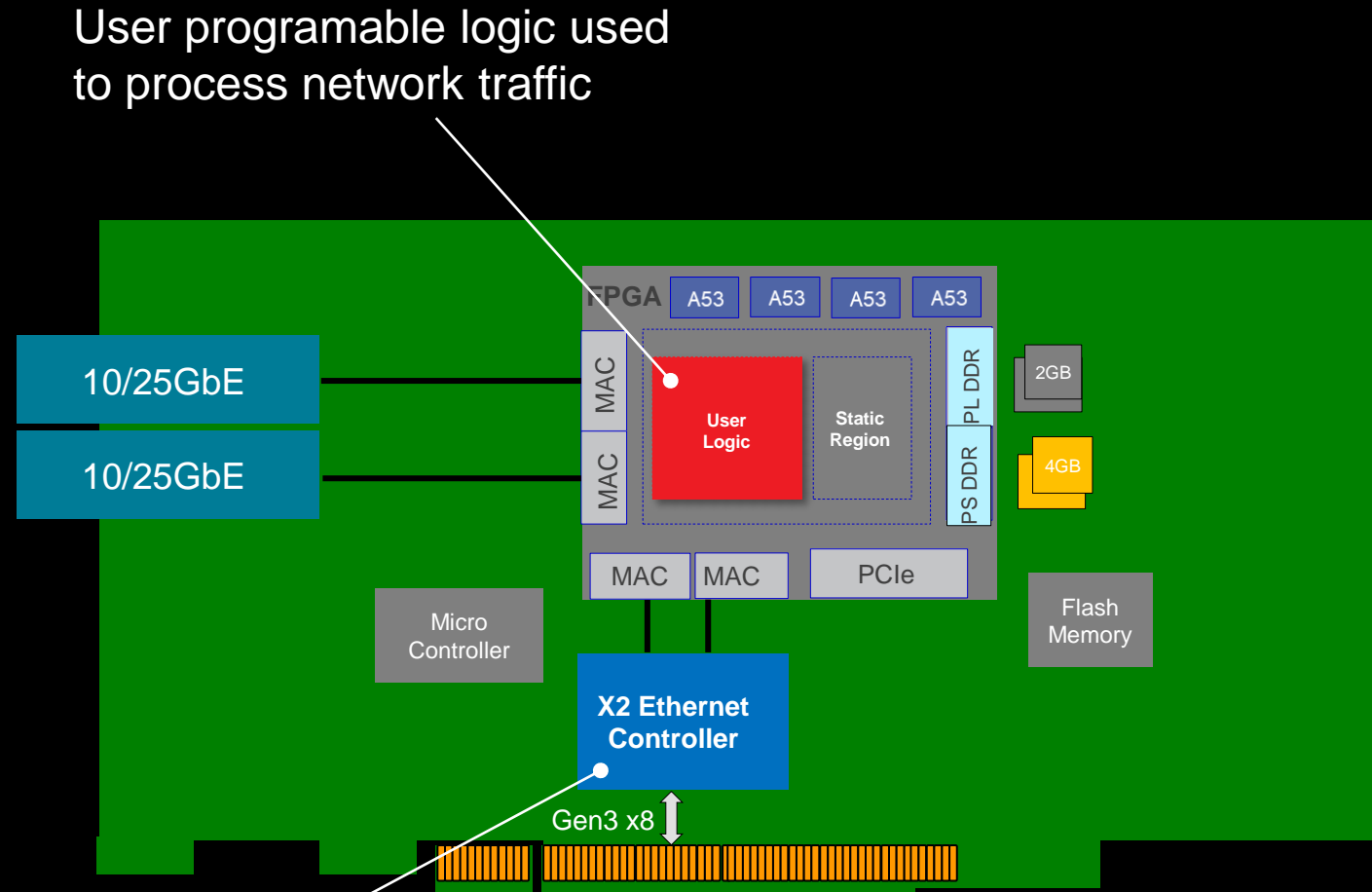
Inline Processing of Network Traffic with FPGAs

May 2022

FPGAs deployed as bump in the wire to process network data, reducing CPU traffic by 50%



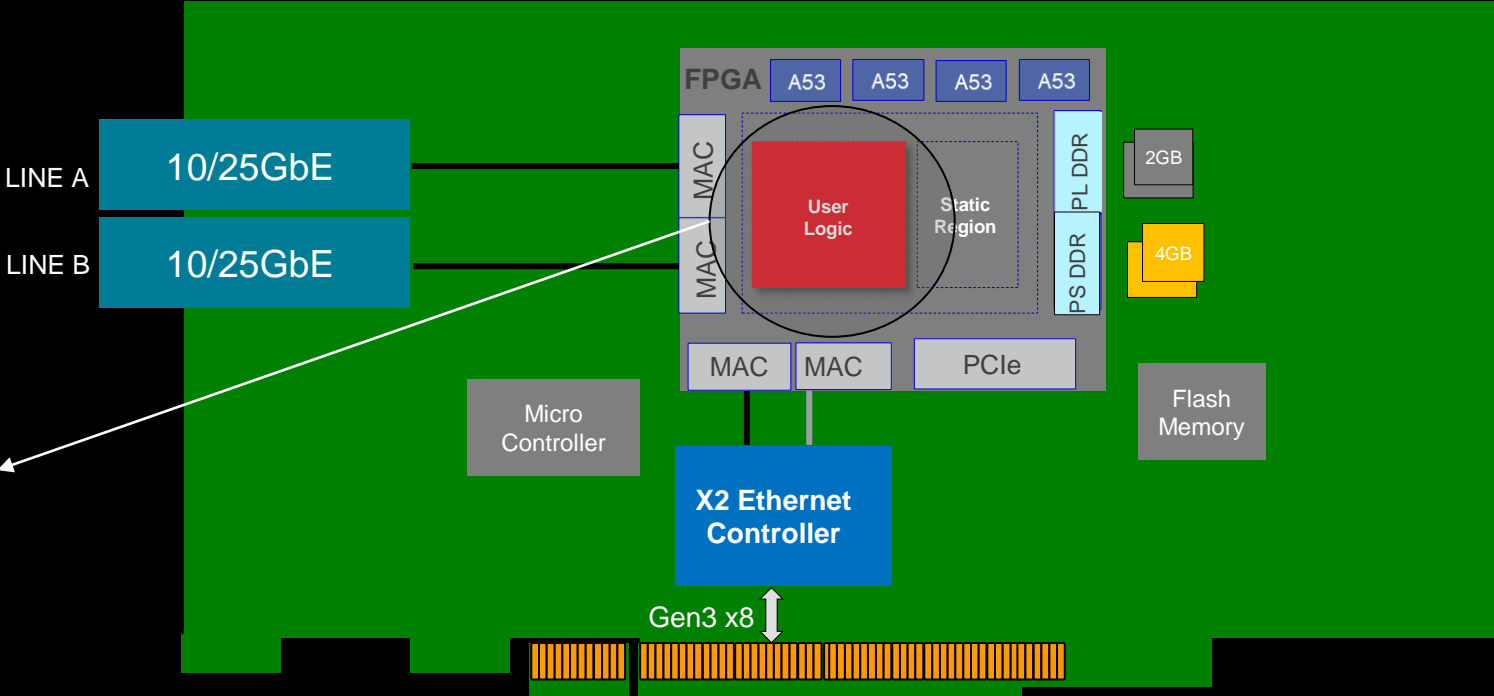
U25N Block Diagram



User programable logic used to process network traffic

Same functionality as X2522 low latency NIC

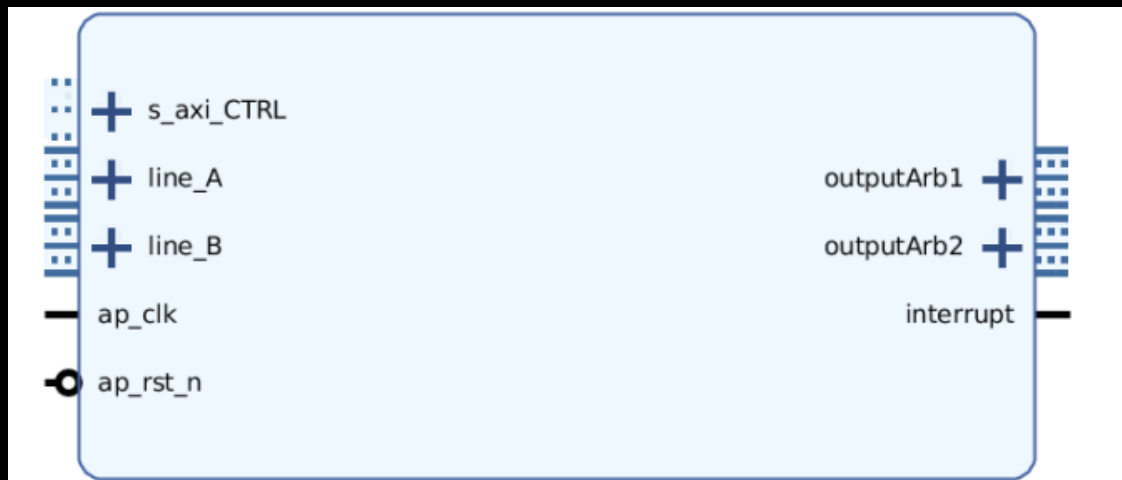
Inline Processing Example to Reduce Network Traffic: Line Arbitration



Line A	1	2			3	4		5
Line B	1		2	3			4	
Output	1	2		3		4		5

Bandwidth halved at the output of the line arbitration module

Software Development Flow to Create the Inline Plugin

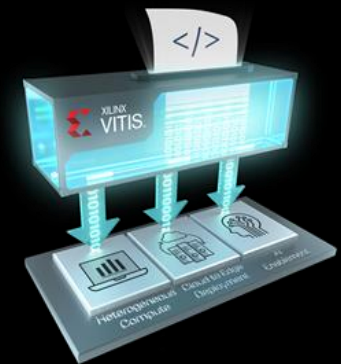


High level programming language (C++) used to implement line arbitration using Vitis



Software Platform

Fully customizable using standard libraries and C/C++





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