STAC Update: FPGA SIG

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FPGA SIG background

- Founded with 7 financial firms
- Goal:
  - Work together on non-proprietary challenges in FPGA development that all firms would benefit from solving
- Initial objectives
  - Facilitate dialog regarding common challenges in FGPA design, development, testing and deployment
  - Articulate industry requirements for FPGA hardware and toolchains where commonalities exist

What's happening now

- The group is meeting every 4 to 6 weeks
- Grown to
  - 16 financial firms
    - Exchanges, hedge funds, prop shops, and banks
  - 7 vendors
    - board, chip, development tools, and IP providers
    - vendors who leverage FPGA for their own projects
- Expanding on initial objectives, with focuses on:
  - Joint initiatives that allow for collaboration across financial firms and vendors
  - Exploring open source and open-source friendly projects
  - Deeper dives with vendors on critical tool chain components

Current collaborations

- In August and September, the group agreed to start collaborations on three main projects
- RapidWright / RapidStream improvements, including
  - Common requirements, requests, and prioritized bugs
  - Collaborating with developers at AMD at a deeper level
- Language support
  - Jointly contribute to VHDL and SystemVerilog projects that check canonical language feature support in other tools
  - Use to convey of critical features to vendors
- Joint development of open-source Switch and/or NIC reference implementation
  - Currently scoping the project
  - Exploring currently existing projects as starting points

FPGA SIG update

- Next meeting will take place in November
- Smaller groups focusing on each collaboration
- You too can join us

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