Gateware Defined Networking (GDN) for Ultra Low Latency Trading and Compliance

STAC Summit: Panel: FPGA for trading today: December 2015

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GDN Powers Algo-Logic IP Cores, Pre-built FPGA Applications, and Systems

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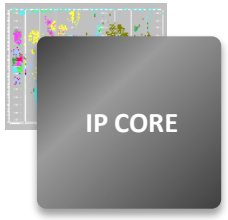
GDN

Gateware Defined Networking

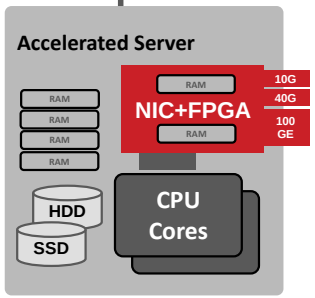


Low Latency MAC,TCP, Protocol Parsers Order Book cores

Pre-Programmed apps in multiple FPGA vendor devices

Pre-Programmed apps in multiple FPGA Cards

Integrated Switch Solutions

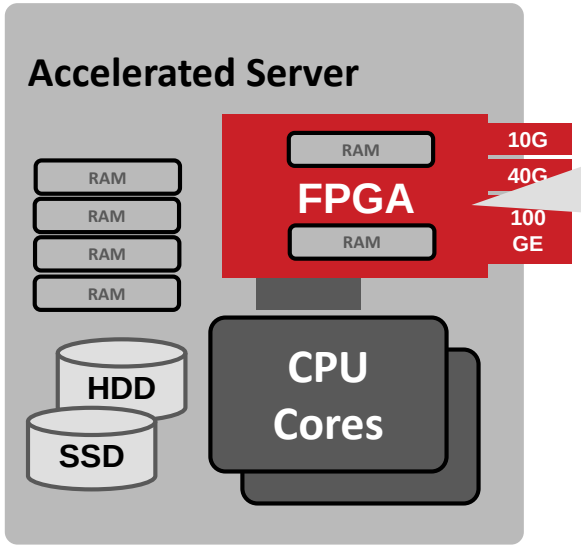


Integrated Server Systems

Data Center Deployments to Co-Location Facility

Algo-Logic's Family of Accelerated Finance Applications

- **Tick-to-Trade System**
- **Low Latency Library**
- **Full Order Book**
- **Low Latency TCP**
  - 76 ns MAC to Application
- **10GE PHY/MAC**
  - 89 ns Round-trip latency
- **Market Data Filter**
- **Protocol Parsers**
  - All major exchanges

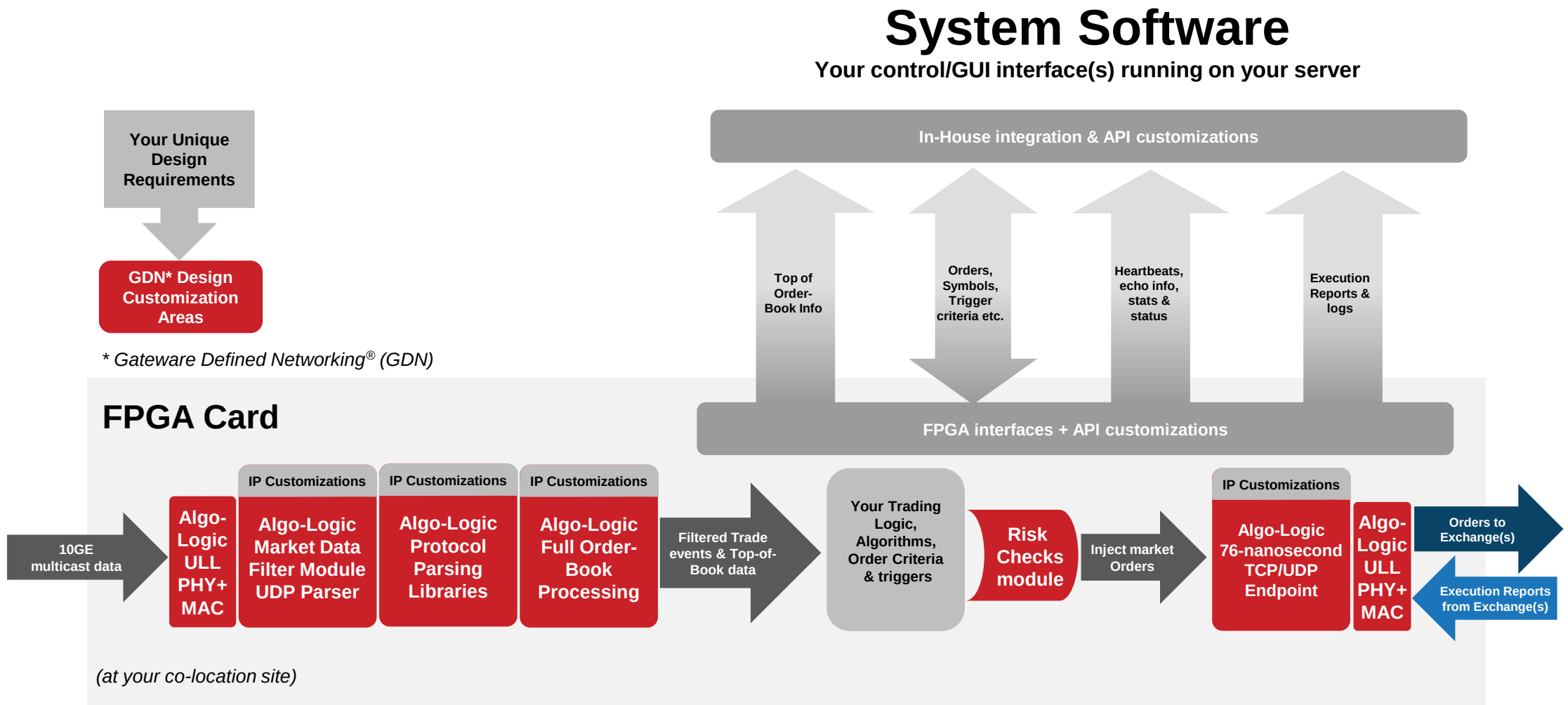


Algorithms in Logic:

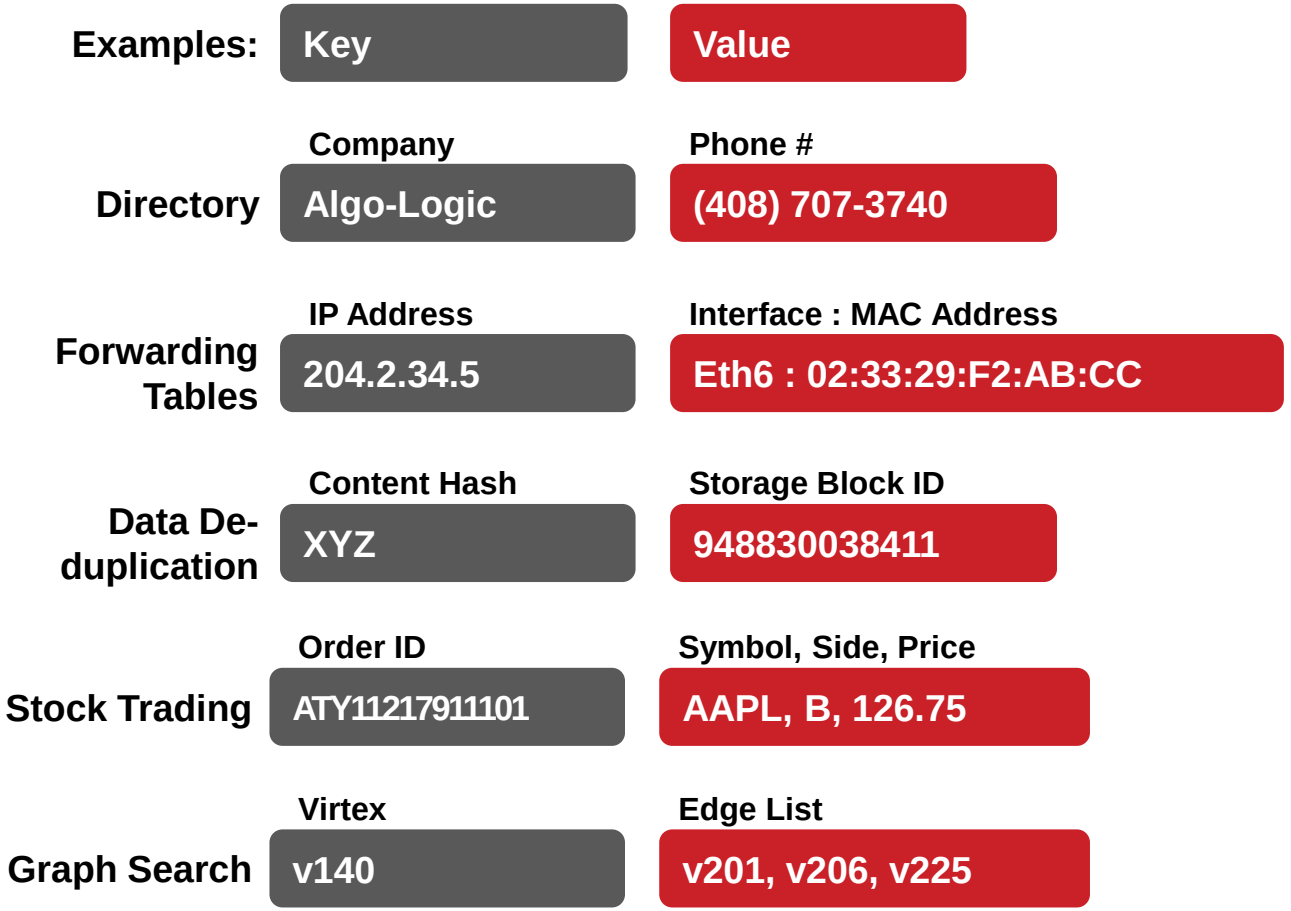
All apps run in FPGA

Not STAC Benchmarks

Algo-Logic's Tick-to-Trade System: Full Offload to FPGA



Algo-Logic's Key Value Store (KVS)

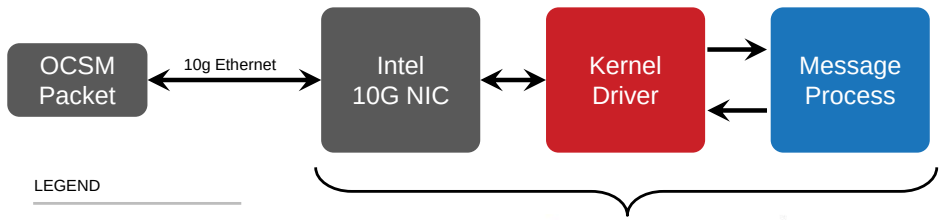


- **Key/Value Store (KVS)**
  - Simplifies implementation of large-scale distributed computation algorithms
  - Data Center Servers exchanges data over standard Ethernet
- **Challenges**
  - Operating System delays packets and limits throughput
  - Per-core processing inefficient at high-speed packet processing
- **Solutions**
  - Bypass kernel bypass with DPDK
  - Offload of packet processing with FPGA

Implementation of KVS with Socket I/O, Kernel Bypass, and GDN in FPGA

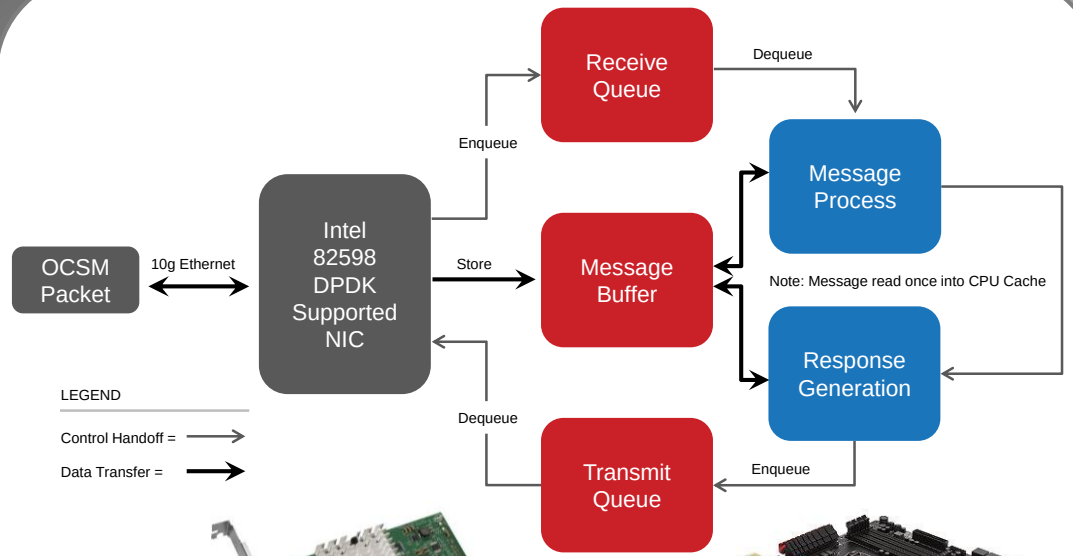
- **Benchmark same application**
  - Key/Value Store (KVS)
- **Running on the same PC**
  - Intel i7-4770k CPU, 82598 NIC, and Altera Stratix V A7 FPGA
- **With three different implementations**
  - Socket I/O, Kernel bypass with DPDK, FPGA

Traditional Socket I/O



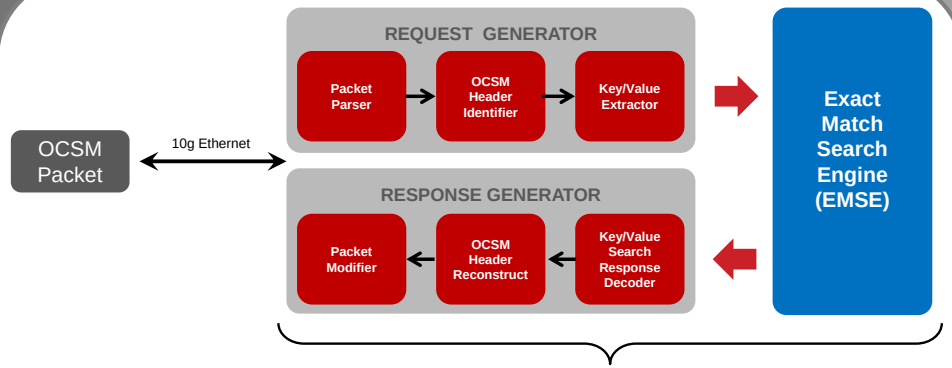
Algo-Logic software on Intel 82598 10GE NIC and Core i7-4770k CPU

Kernel Bypass with DPDK



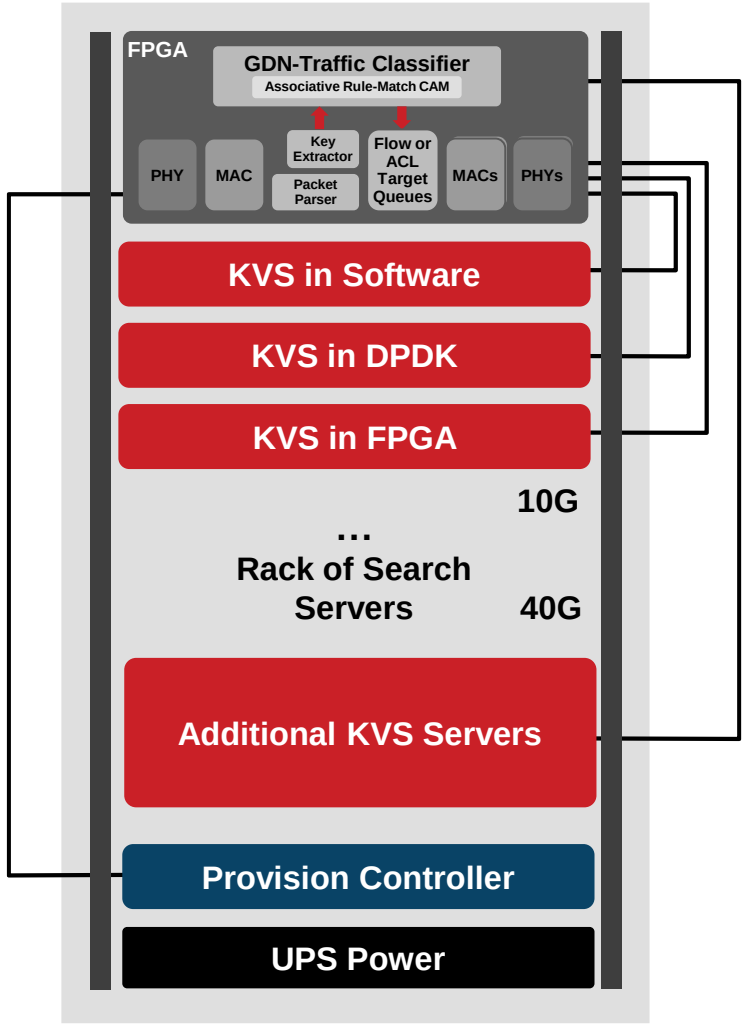
Algo-Logic software on Intel 82598 10GE NIC and Core i7-4770k CPU

GDN in FPGA



Algo-Logic gateware on Nallatech P385 with Altera Stratix V A7 FPGA

Measured Latency, Throughput, and Power Results



All Datapaths Summary	Latency (µseconds)	Tested Throughput (CSMs/sec)	Power (µJoules/CSM)
Sockets	41.54	4.0	11
DPDK	6.434	16	6.6
RTL	0.467	15	0.52

All Datapaths Summary	Latency (µseconds)	Maximum Throughput (CSMs/sec)	Power (µJoules/CSM)
GDN vs. Sockets	88x less	13x	21x less
GDN vs. DPDK	14x less	3.2x	13x less

Advance Results: http://algo-logic.com/KVS-whitepaper

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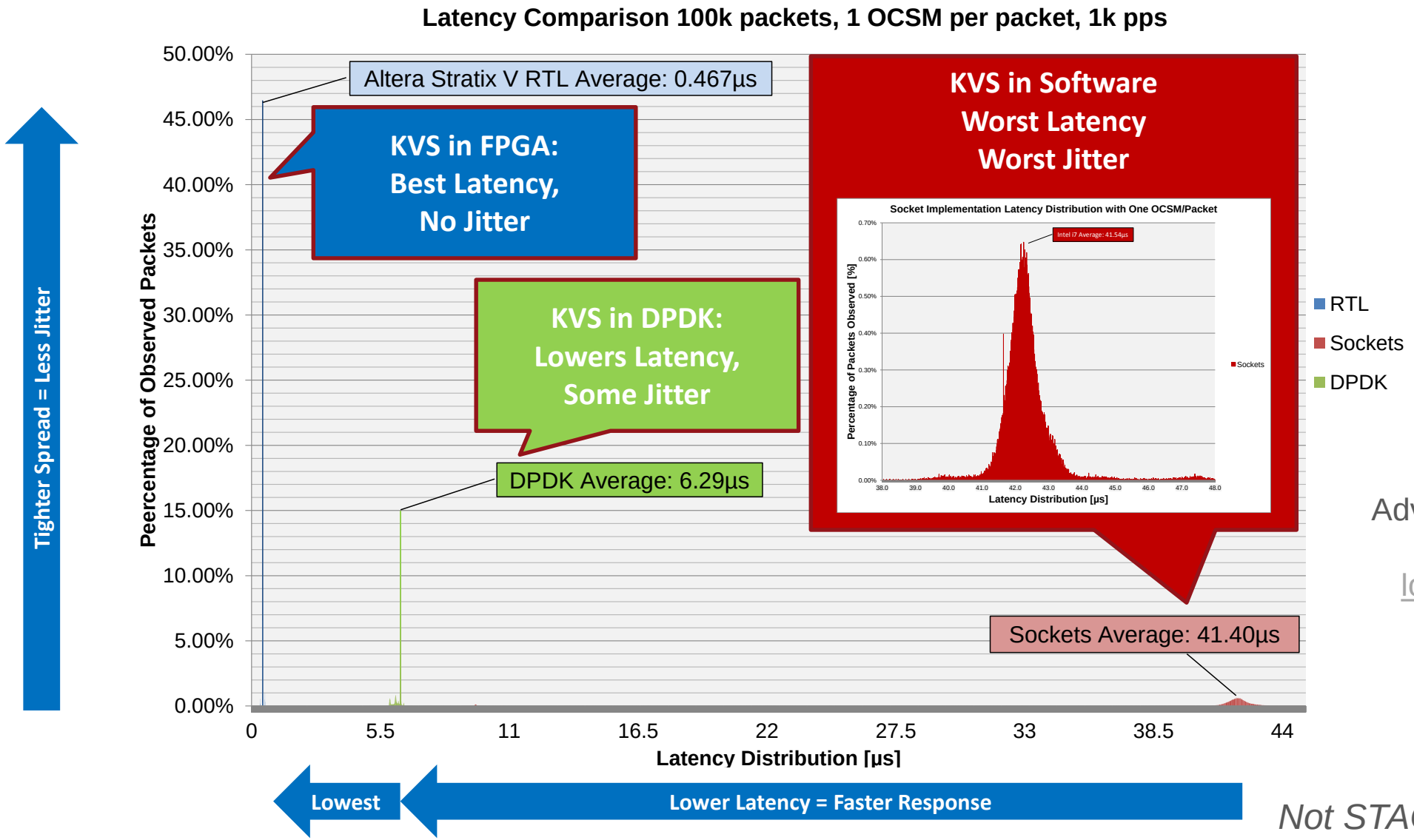
KVS Latency in FPGA, DPDK, and Sockets



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Key Results: Gateware Defined Networking®

Gateware Defined Networking® (GDN)

- **Lowers Latency**
  7x to 45x over optimized DPDK and traditional Linux networking software

- **Increases Throughput**
  3x to 13x improvement in Throughput / Server

- **Reduces Power**
  13x to 21x less Power / Server

Advance Results:
http://algo-logic.com/KVS-whitepaper

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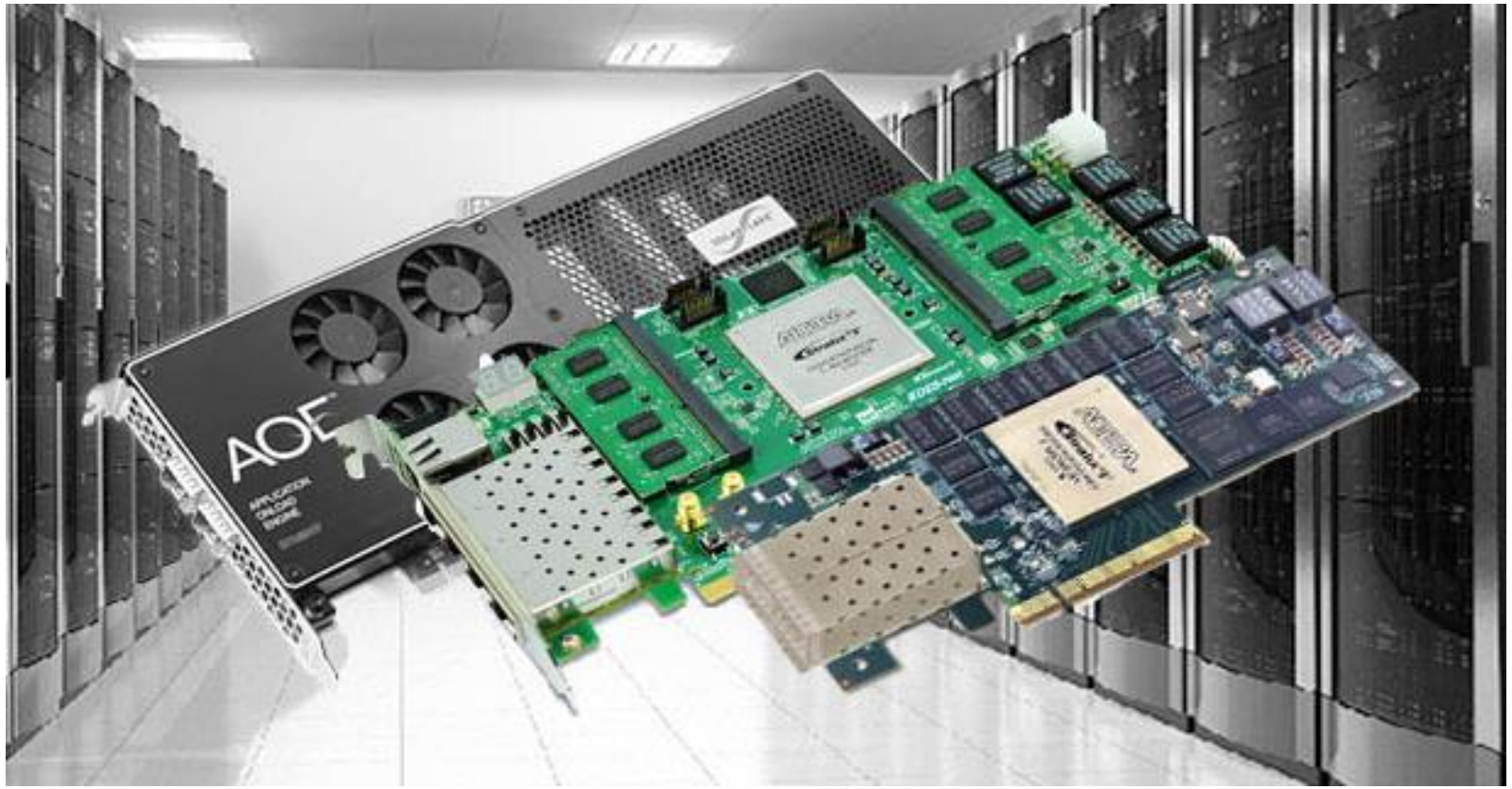
Algo-Logic is Partnered to Provide Solutions on All Major Platforms



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Thank You!

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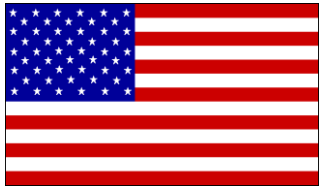

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