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Low Latency Tick-to-Trade System with new support for CME SBE MDP3

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Presented at STAC, Chicago

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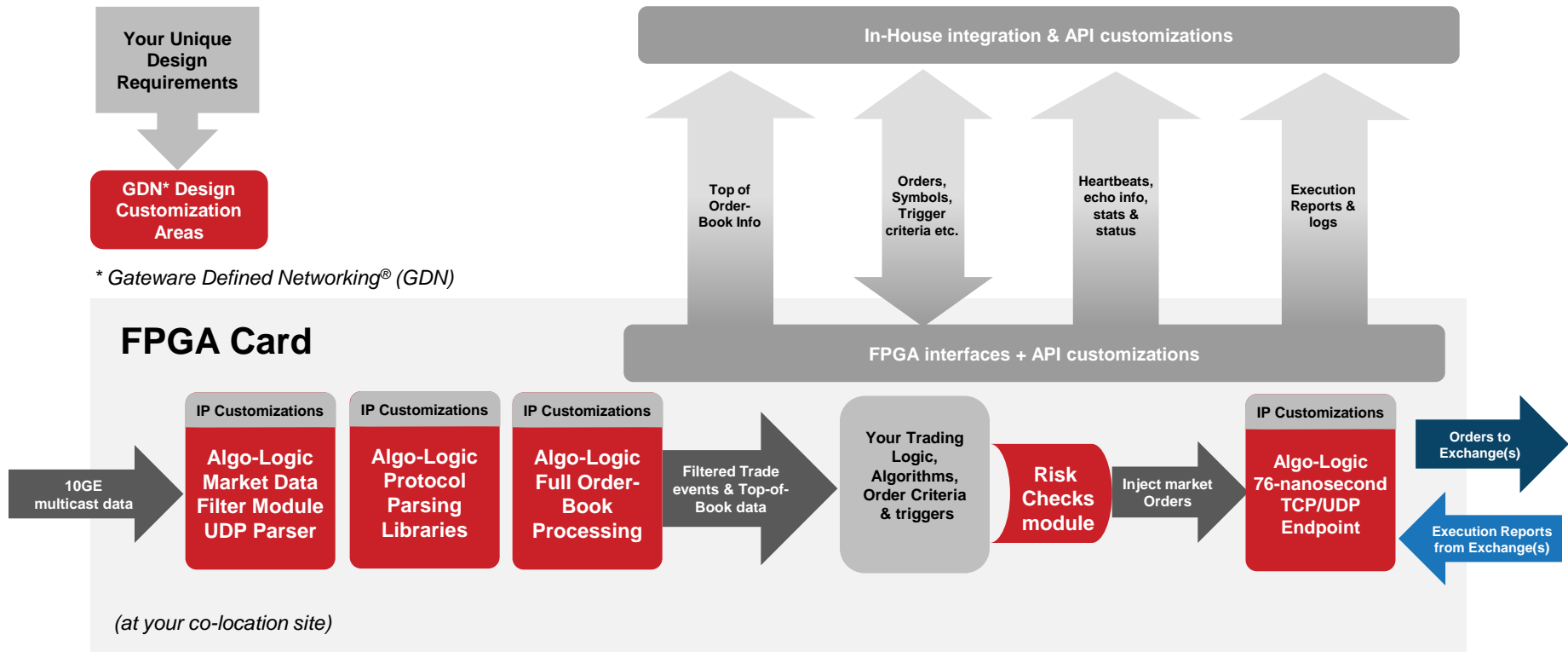
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New Announcement Today

- **Support for CME SBE MDP3**
  - FPGA-accelerated decode of binary market data
  - Replaces FAST FIX decoding
  - Lower latency due to smaller messages sizes and binary data

- **Augments existing Tick-to-Trade (T2T) FPGA components for**
  - Protocol parsing
  - Market data filter
  - Order book
  - Customer-proprietary trade logic
  - Customer provided risk checks
  - 89ns 10GE PHY/MAC with 76ns TCP Endpoint

- **Achieves Sub-microsecond Tick-to-Trade Latency**
  - Though not (yet) a STAC benchmark

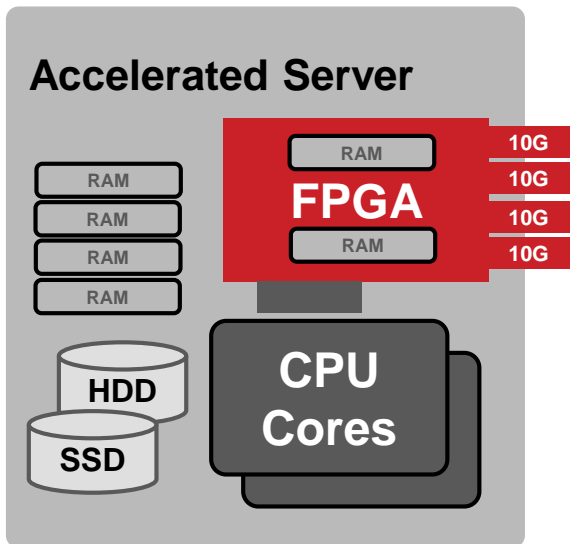ALGO-LOGIC.

Ultra Low-Latency FPGA Tick-to-Trade System

System Software
Your control/GUI interface(s) running on your server

Your Unique Design Requirements

GDN* Design Customization Areas

* Gateware Defined Networking® (GDN)

In-House integration & API customizations

Top of Order-Book Info

Orders, Symbols, Trigger criteria etc.

Heartbeats, echo info, stats & status

Execution Reports & logs

FPGA Card

FPGA interfaces + API customizations

IP Customizations — **Algo-Logic Market Data Filter Module UDP Parser**

IP Customizations — **Algo-Logic Protocol Parsing Libraries**

IP Customizations — **Algo-Logic Full Order-Book Processing**

10GE multicast data

Filtered Trade events & Top-of-Book data

Your Trading Logic, Algorithms, Order Criteria & triggers

Risk Checks module

Inject market Orders

IP Customizations — **Algo-Logic 76-nanosecond TCP/UDP Endpoint**

Orders to Exchange(s)

Execution Reports from Exchange(s)

(at your co-location site)

FPGA Accelerated Server

- **FPGA Augments Existing Servers**
  - Can run on an expansion card (same size as a GPU)
- **Tick-to-Trade Application runs on FPGA**
  - Implements low-latency Tick-to-Trade Application
  - Without assistance from CPU cores on time-critical path

Accelerated Server

| RAM |
| RAM |
| RAM |
| RAM |

RAM
FPGA
RAM

10G
10G
10G
10G

HDD
SSD

CPU Cores

ALGO-LOGIC

2U Rack Server

ALGO-LOGIC.

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