'Hardware Acceleration Today'
Full Order-Book FPGA

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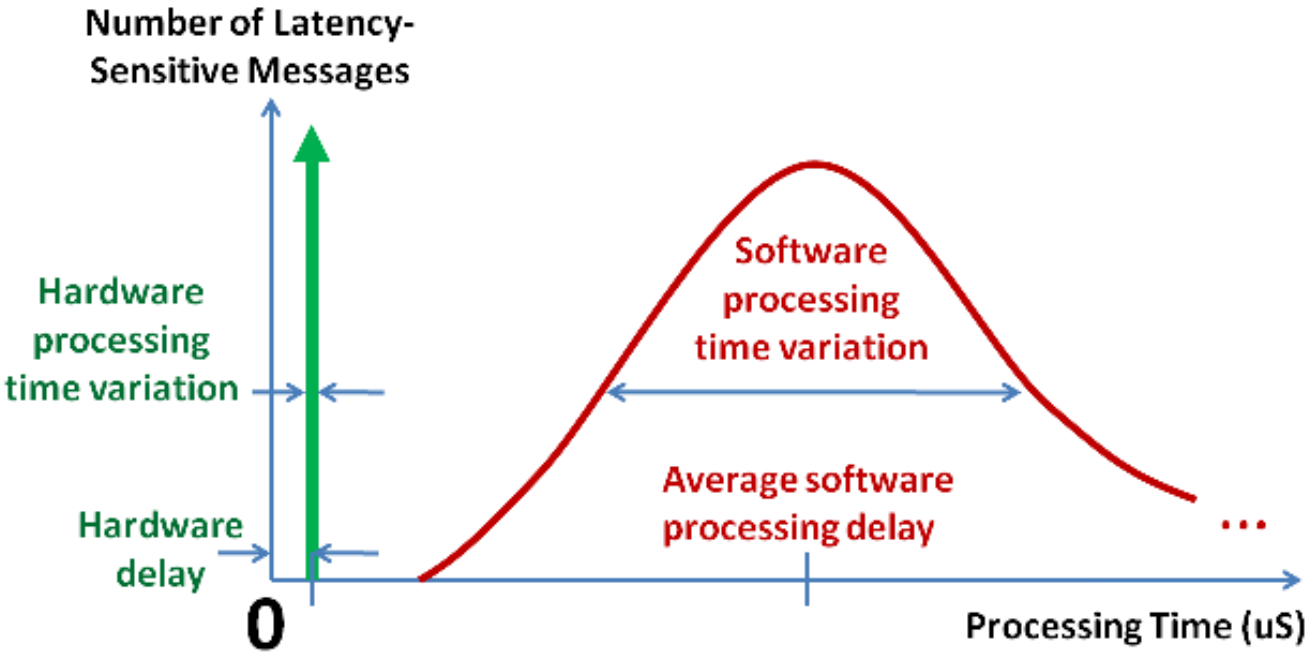
Latency & Jitter: Hardware vs Software

- **Algo-Logic's FPGA Gateware Solutions**
  - Lowest Latency due to implementation in FPGA hardware
  - No Jitter because circuit uses constant # of clock cycles
- **Software**
  - PCI bus delays + Cache jitter + process scheduling + …



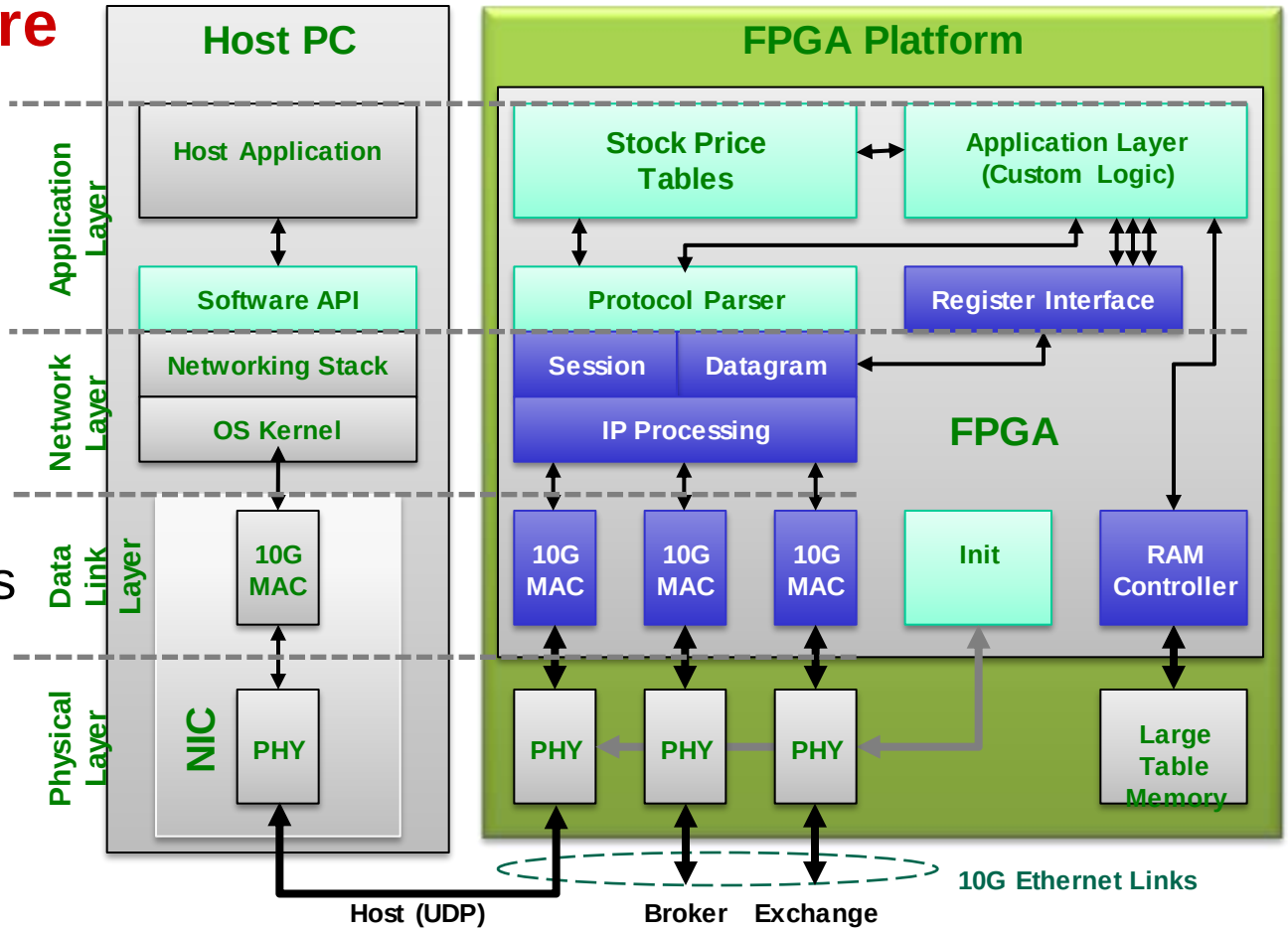
Algo-Logic's Gateware® Infrastructure

Dedicated Hardware

- TCP Sessions
  - Order Processing
- UDP Datagrams
  - Market Data Feed
- Protocol Parsing
  - OUCH, ITCH, ArcaDirect, FIX, LSE, XPRS, …
- Trading Applications
  - Risk Checks
  - Order Injection
  - Tick-to-Trade Apps
  - Order Book

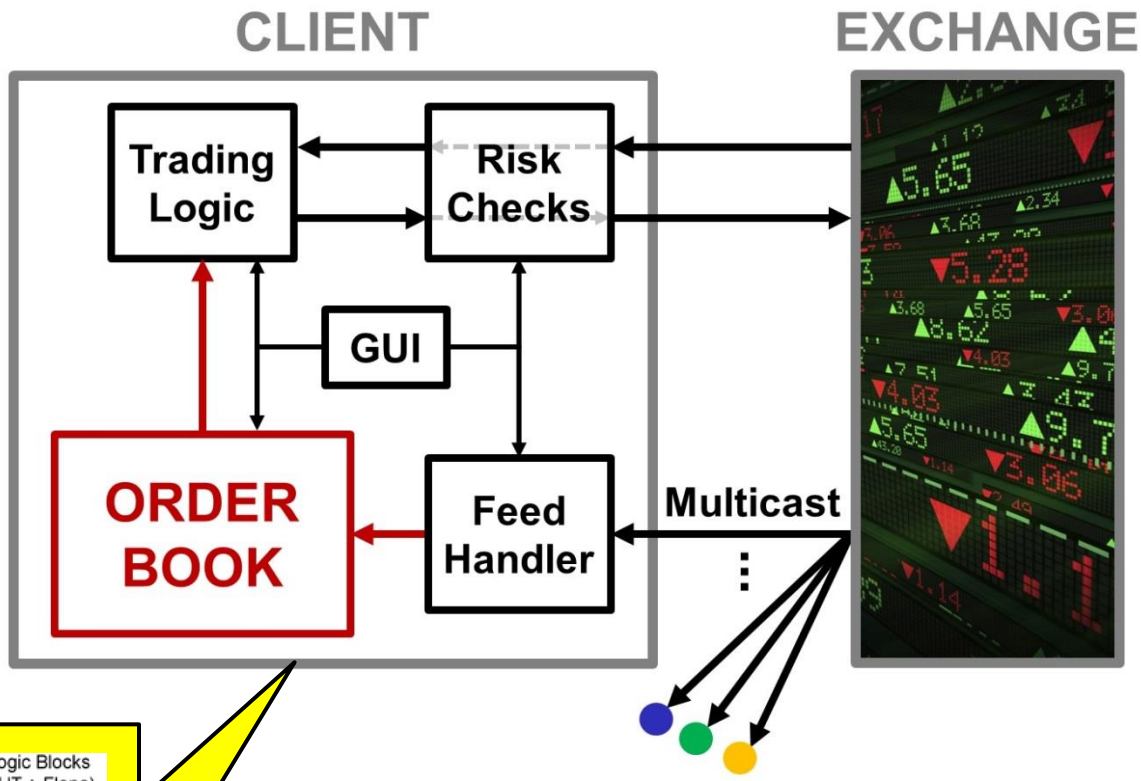
Software

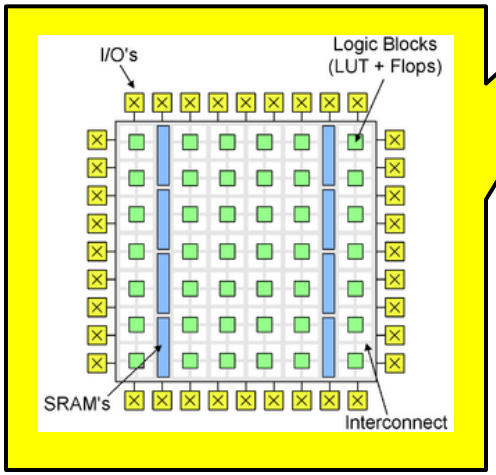
- Control API
- GUI Configuration
- Monitoring



All of Algo-Logic's latency-critical processing is in pure hardware

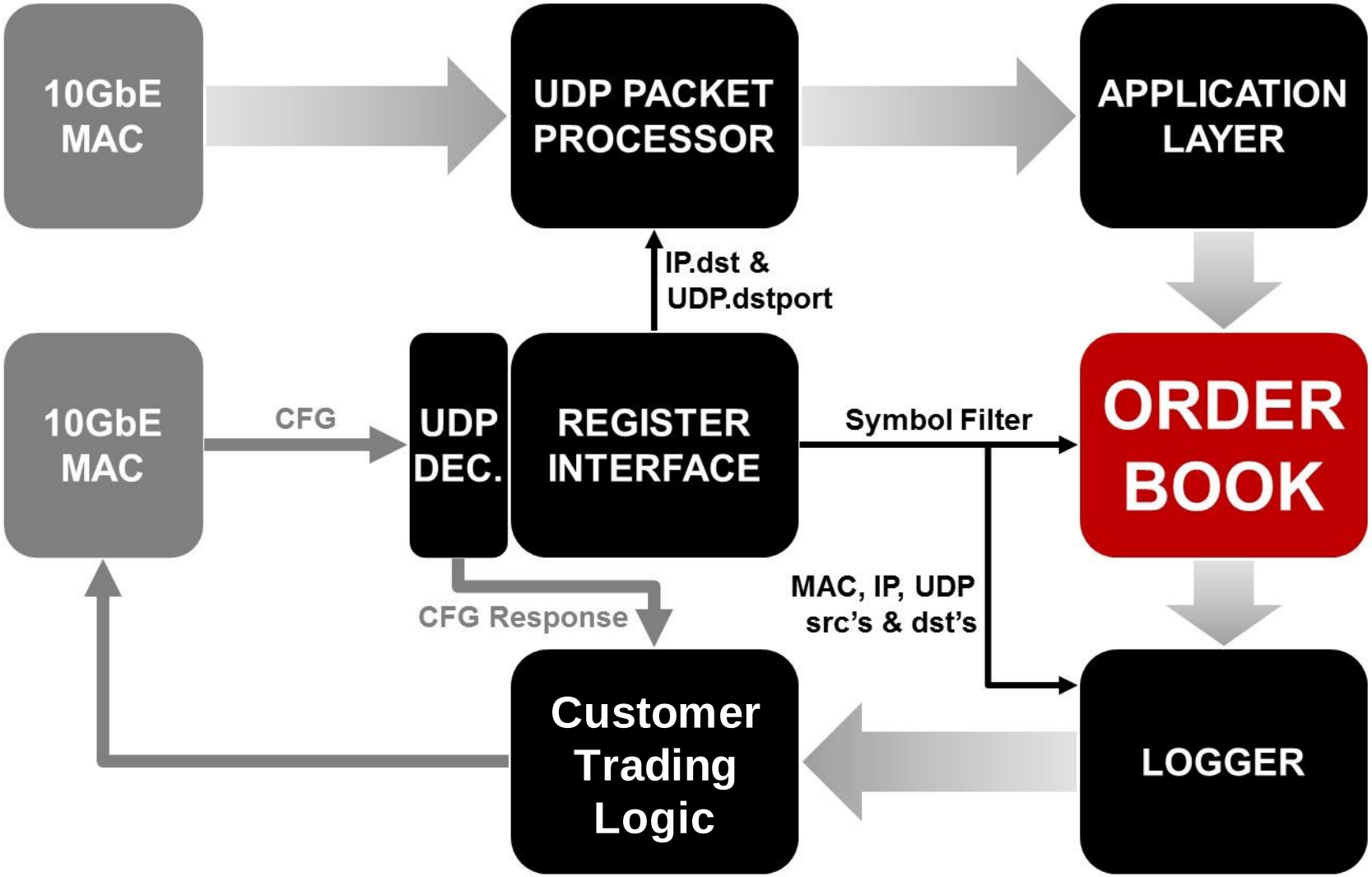
Algo-Logic's Tick-to-Trade Solutions





Full Solution in FPGA Gateware

Algo-Logic's Order-Book: Pure Logic

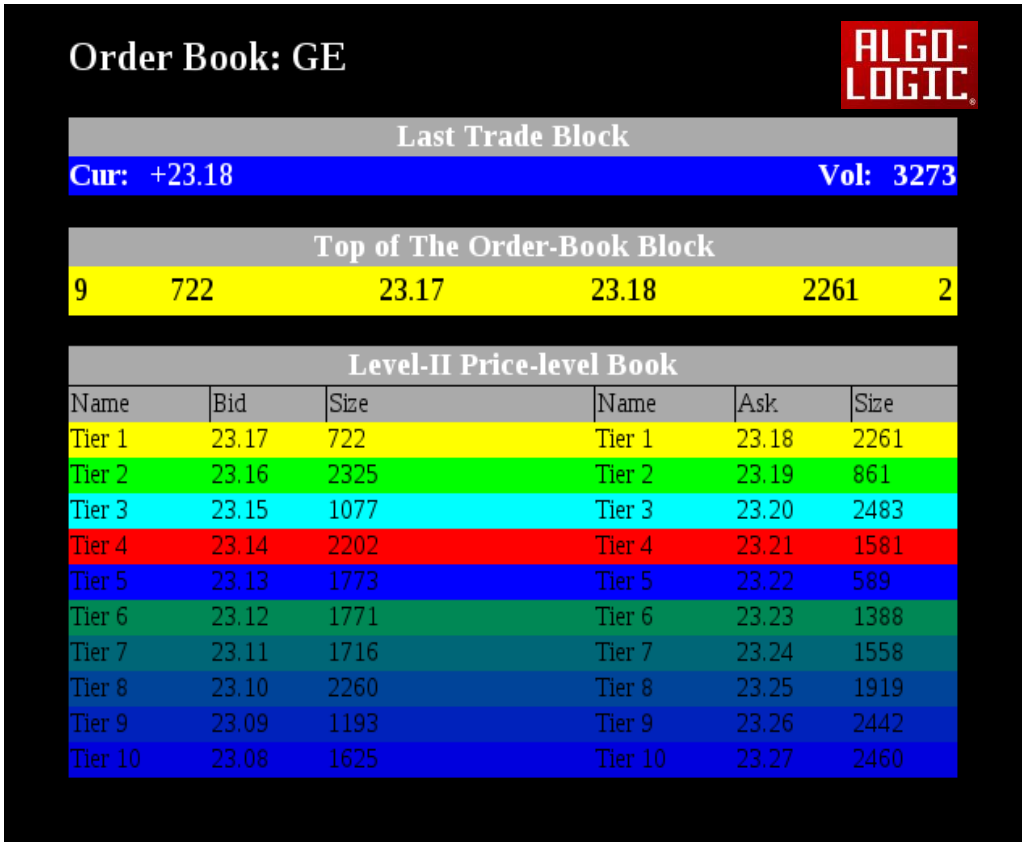


Key Features: Algo-Logic Order Book

- **Stream-based Output from FPGA core**
  - Can operate as a core inside a single FPGA solution
  - Interfaces directly to customer's proprietary algorithmic trading strategies
  - Compatible with any downstream processing logic or software application
- **L-2 Output**
  - Default size of 10 price-levels per symbol
    - Fully scalable to larger sizes
    - Configurable by the user via API
- **L-3 Order-Book updates complete**
  - Complete with processing latency < 450 ns
- **Combined L-3 + L-2 Order-Book**
  - Complete with processing latency < 1 µs

Not STAC Benchmarks

Output of Algo-Logic Order Book



Order Book: GE

ALGO-LOGIC

Last Trade Block					
Cur: +23.18				Vol: 3273	

Top of The Order-Book Block					
9	722	23.17	23.18	2261	2

Level-II Price-level Book					
Name	Bid	Size	Name	Ask	Size
Tier 1	23.17	722	Tier 1	23.18	2261
Tier 2	23.16	2325	Tier 2	23.19	861
Tier 3	23.15	1077	Tier 3	23.20	2483
Tier 4	23.14	2202	Tier 4	23.21	1581
Tier 5	23.13	1773	Tier 5	23.22	589
Tier 6	23.12	1771	Tier 6	23.23	1388
Tier 7	23.11	1716	Tier 7	23.24	1558
Tier 8	23.10	2260	Tier 8	23.25	1919
Tier 9	23.09	1193	Tier 9	23.26	2442
Tier 10	23.08	1625	Tier 10	23.27	2460

As viewed from GUI Display

- **Contents**
  - Last Trade
    - Price & Size
  - Top of Book
    - Best Bid & Ask
  - Sorted list of size N
    - Top Bids: Price & Size
    - Top Asks: Price & Size
- **Available as:**
  - AXI-4 Stream or Avalon Bus
    - for processing in FPGA
  - UDP/IP Packet
    - for processing in software
  - And/or: GUI Display
    - for verification and demonstration

Full Order-Book Product Specifications & Performance

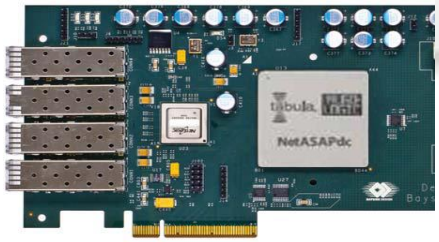
Parameter	Value
Order-Book EMSE2 IP-Core Search Rate	150 Million Searches per Second (MSPS) @ 10Gbps
Application	Filtered Symbols, Position, Order-Book Best Bid/Ask & Level-II calculations
Default L-2 Book Price Levels	10+ scalable
Deep L-3 Table Option	Yes – fully scalable with Hybrid & Off-Chip DDR3/QDRII memory
Memory Footprint	~5.0% in Stratix V A7
L-3 Book Default Build/Refresh rate	Every 250 nanoseconds
L-3 Book processing Time	< 450 nanoseconds
Total L-3 + L-2 Books Processing Time	< 1.0 micro-second
FPGA Devices Supported	Altera V, Virtex-7
FPGA Platforms Supported	PLDA/Accelize XP5, Terasic DE5Net, Nallatech P385, Bittware S5PH-Q, Solarflare AOE

Algo-Logic's Cross-Platform Solutions

- **Devices**
  - Apps synthesize across multiple FPGA

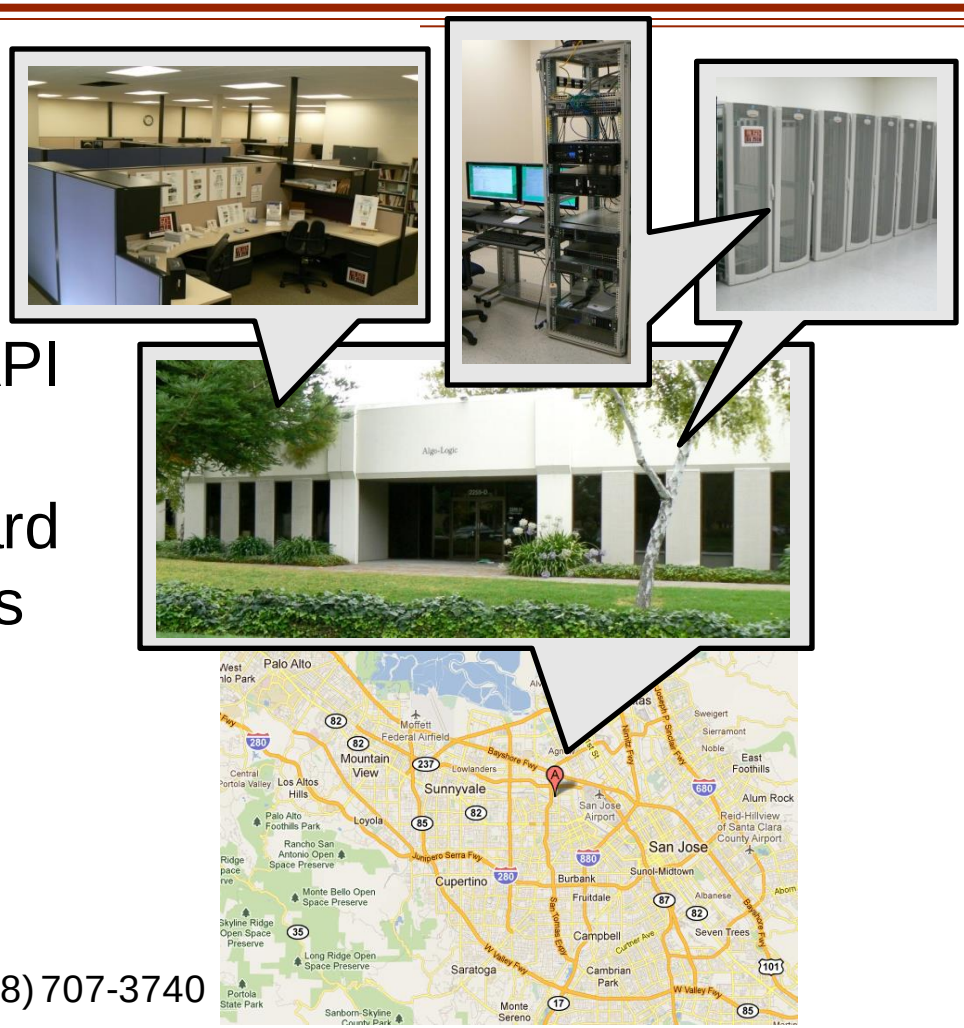
ALTERA® XILINX® tabula

- **Platforms**
  - Gateware Solutions run on multiple platforms



Conclusions

- **Algo-Logic's Gateware**
  - Offloads all time-critical processing to FPGA
  - Provides simple software API for control & configuration
  - Runs on all major FPGA card and switch vendor platforms
- **Order-Book**
  - Tracks all orders
  - Output 10 Levels
  - L3 Processing
    - < 450ns
  - L2+L3 Latency
    - < 1.0 uS



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