STAC Update:
Fast Data

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FPGA SIG: background

- Finance has pioneered the use of FPGA as network-attached compute
- Today FPGA use in finance is diverse, including:
  - Accelerated network I/O
  - Market data processing
  - Execution of realtime trading logic
  - Pre-trade risk computation
- For years, STAC has measured the benefits of FPGA
- For years, STAC has been the place to discuss the challenges of FPGA
- Last year, the STAC FPGA SIG started taking action on the challenges

FPGA SIG: background

- Currently 12 financial firms, including:
  - Exchanges
  - Dealers
  - Proprietary trading firms
  - Hedge funds
- Looking to work with more vendors
  - More on this in a bit
- Group's current focus:
  - Facilitate dialog on common challenges in design, development, testing and deployment
  - Articulate industry requirements for hardware and toolchains where commonalities exist

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Survey: FPGA hardware needs

- Financial firms are often early requesters / early adopters
- But there are two issues:
  - FPGA device and board manufacturers provide solutions for a variety of industries
  - FSI needs are frequently expressed one firm at a time
- This survey is a first step in identifying common FSI FPGA hardware needs
  - Both current and future
- Aggregated results will amplify the FSI voice to hardware providers
  - Goal is to influence their roadmaps

Protecting respondents' identities

- The survey will **not** collect information identifying individuals or firms
- Will use the same methodology as previous STAC surveys (e.g., time sync) to ensure anonymity without duplication
  - Coordinating through your main Council reps
- Results will **not** be presented at the level of individual responses
  - STAC will present all results as aggregations
  - No member of the FPGA SIG will see individual responses

What is on the survey

- Understand basic needs and use
  - Capacity constraints
  - Benefits derived from FPGA (latency vs throughput vs determinism)
  - Broad categories of use
- Focus on needs over the next 3 to 5 years:
  - Hardware
  - IP

Survey report

- Aggregate results with explanatory color
- Will be available to survey respondents
  - Yes, even while remaining anonymous
- FPGA SIG will use it to inform discussions with hardware providers

Taking the survey

- Survey will be live in November 2021
- STAC will reach out to STAC member firms with info on how to participate
- To ensure your voice is heard:

council@STACresearch.com

Development toolchain

FPGA SIG is collaborating to improve the FPGA development lifecycle in 3 ways:

1. Language-feature validation tools:
   - Picking open-source tools to support (both Verilog and VHDL)
   - Contributing important checks to those tools
   - Using collective weight of group to push for use by toolchain vendors
2. New open-source projects in development toolchain
   - The what and how is being discussed in FPGA SIG meetings this winter
3. Working with vendors to open up APIs to make toolchain development easier

- If you are interested in participating, join the SIG:

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FPGA SIG: Next steps

- More direct involvement of vendors, including:
  - Hardware providers
  - Tooling providers
  - Functionality providers
- Will still have occasional meetings with only financial firms
- Always looking for more financial firms to participate in:
  - The main FPGA SIG
  - The toolchain sub-group
  - The hardware sub-group
  - Other future initiatives

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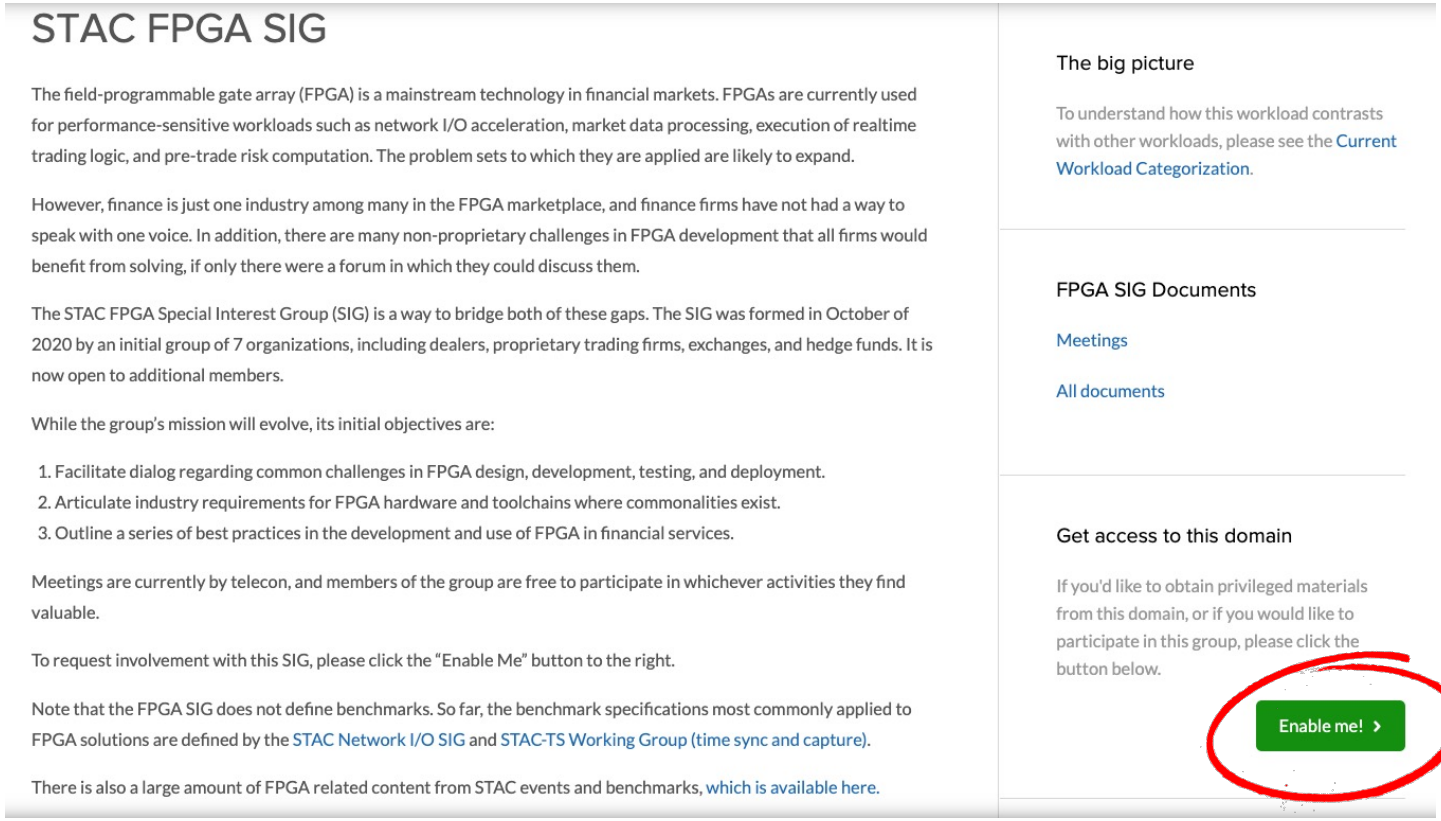
Join the FPGA SIG

Visit www.STACresearch.com/FGPA



STAC FPGA SIG

The field-programmable gate array (FPGA) is a mainstream technology in financial markets. FPGAs are currently used for performance-sensitive workloads such as network I/O acceleration, market data processing, execution of realtime trading logic, and pre-trade risk computation. The problem sets to which they are applied are likely to expand.

However, finance is just one industry among many in the FPGA marketplace, and finance firms have not had a way to speak with one voice. In addition, there are many non-proprietary challenges in FPGA development that all firms would benefit from solving, if only there were a forum in which they could discuss them.

The STAC FPGA Special Interest Group (SIG) is a way to bridge both of these gaps. The SIG was formed in October of 2020 by an initial group of 7 organizations, including dealers, proprietary trading firms, exchanges, and hedge funds. It is now open to additional members.

While the group's mission will evolve, its initial objectives are:

1. Facilitate dialog regarding common challenges in FPGA design, development, testing, and deployment.
2. Articulate industry requirements for FPGA hardware and toolchains where commonalities exist.
3. Outline a series of best practices in the development and use of FPGA in financial services.

Meetings are currently by telecon, and members of the group are free to participate in whichever activities they find valuable.

To request involvement with this SIG, please click the "Enable Me" button to the right.

Note that the FPGA SIG does not define benchmarks. So far, the benchmark specifications most commonly applied to FPGA solutions are defined by the STAC Network I/O SIG and STAC-TS Working Group (time sync and capture).

There is also a large amount of FPGA related content from STAC events and benchmarks, which is available here.

The big picture

To understand how this workload contrasts with other workloads, please see the Current Workload Categorization.

FPGA SIG Documents

Meetings

All documents

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If you'd like to obtain privileged materials from this domain, or if you would like to participate in this group, please click the button below.

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