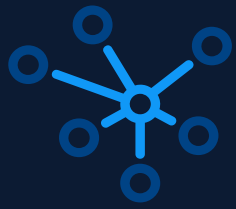


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The Build vs Buy Dilemma Is A False Choice – Market Interaction

May 6, 2021



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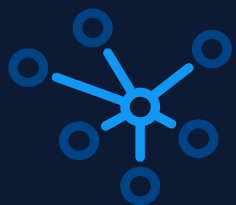
Shōganai

And

"!#"...

*...We All See It
Every Day*

しょうがない



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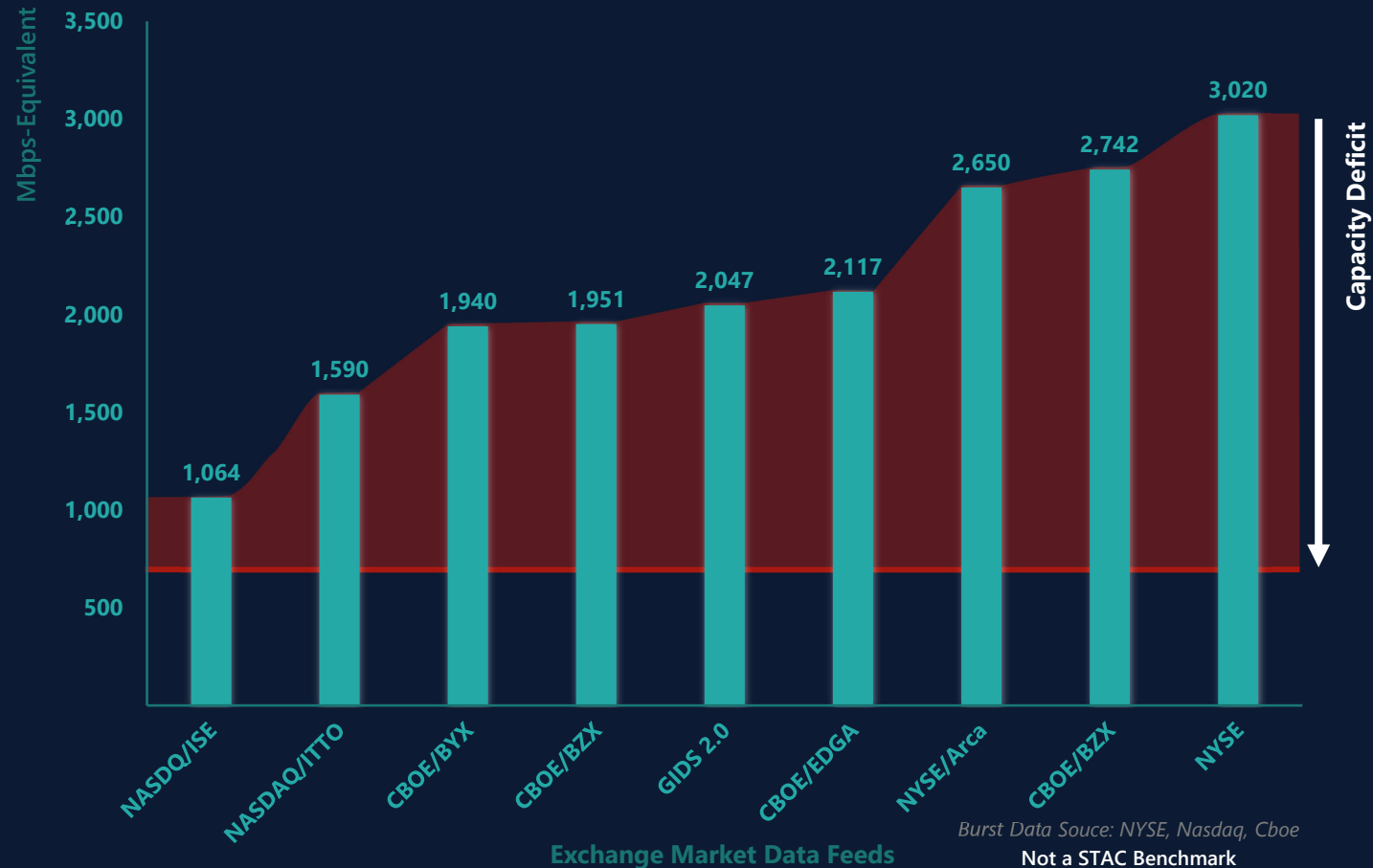
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The Status Quo
Leaves You
Exposed...

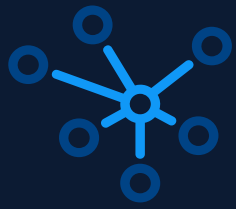
*Typical
Market Data
Burst Rates
Cannot Be
Handled*

10GbE? Line Rate to Software Cannot Be Maintained

1ms Peak Market Data Burst Rate Capacity Requirements



Capability Limitations Bite At The Moment of Peak Risk/Reward



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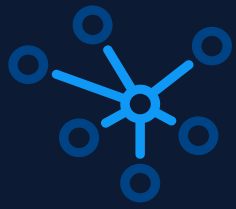
Tougher Than Ever...

...*Buy vs Build Dilemma*

Trading Stack Investment Yields Diminishing Returns

- Today's Trading Stack is **Expensive**
 - *Equipment & People/Co-Lo Real Estate/Energy Usage*
- Today's Trading Stack is **Limiting**
 - *Architecture Constraints/Multiple Hops/Unnecessary Latency*
- Today's Trading Stack is **Compromised**
 - *Regulatory/Exchange/Broker Requirements*
- Today's Trading Stack is **Distracting**
 - *Strategic Differentiation & Buy vs Build*

Strategic Differentiation and Profitability Threatened



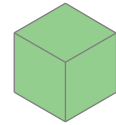
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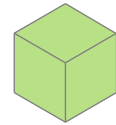
Naros.CCS™
Comprehensive
Connectivity
Solution...

*Modular
Approach To
Optimization*

Naros.CCS™ – Library of Functions



Network
MAC/PCS



Network/Application
Stack, PCIe Transfer, & Kernel Bypass



Network
Expanded Functionality



Packet
Capture & Replay



Packet
PTP & PPS



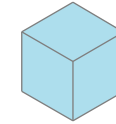
Broker
Validation & Risk Checks



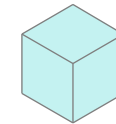
Trading
Multi-Dimension Queue



Trading
Order Transmission



Trading
Lightweight Venue API



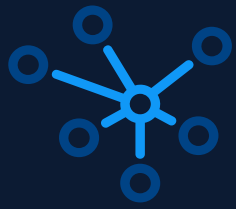
Trading
Market Data Parsing



Trading
Validation & Risk Checks

*Note: Various Embodiments Above, Singly or in
Combination, are Patented and/or Patent Pending*

Library of Individual Functions Available Separately Or In Combination



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How To Optimize...

*When Tools
Are Limited
By The Very
Constraints
They Should
Identify?*

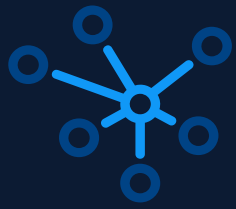
Testing & Measurement Are Essential For Optimization

“Management of a system requires knowledge of the interrelationships between all of the components within the system...”

W. Edwards Deming

“If you can’t measure it, you can’t improve it.”

Peter Drucker



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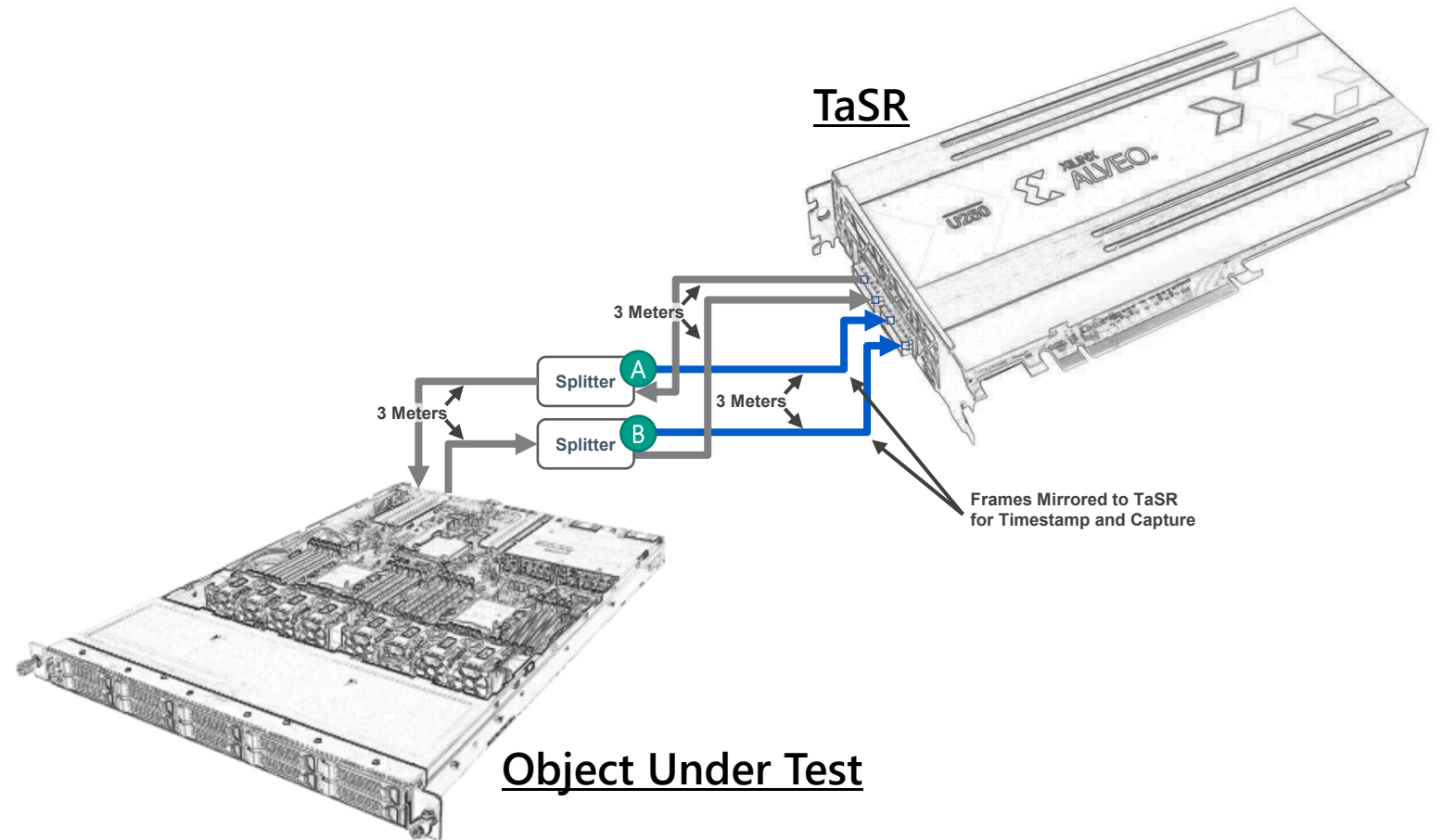
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Expose
Bottlenecks...

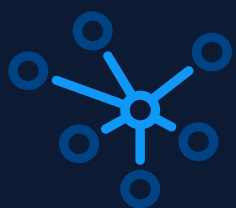
*Realistic
Burst & Stress
Testing of
Application/Network
Performance*

TaSR™ - Hyper-Accurate Testing & Measurement



TaSR™ is an FPGA-Based <5ns-Precision Performance Measurement System

Not a STAC Benchmark



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Expose
Bottlenecks...

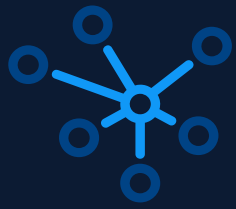
*Realistic
Burst & Stress
Testing of
Application/Network
Performance*

TaSR™ - Hyper-Accurate Testing & Measurement

- RFC 2544 (Ethernet) Compliant Including:
 - Throughput, Burstability, Latency, Frame Loss, System Recovery
- Non-RFC 2544 Functionality Including:
 - Variable Delay, Packet Capture, Replay, Internal Clock Timestamp
- Layer 2 Start-Of-Frame FIFO, FILO, LILO Performance Measurements
- Configurable Traffic Generation (Protocol, Payload, Rate)

TaSR™ is an FPGA-Based <5ns-Precision Performance Measurement System

Not a STAC Benchmark



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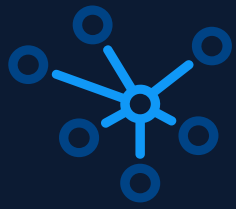
Cut
Through
The
BS...

...To
Focus
On
Differentiation

Trading Stack Investment Revisited

- Today's Trading Stack is **Expensive**
 - *Equipment & People/Co-Lo Real Estate/Energy Usage*
- Today's Trading Stack is **Limiting**
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 - *Strategic Differentiation & Buy vs Build*

Deploy Your Resources To Focus On Differentiating Competitive Advantages



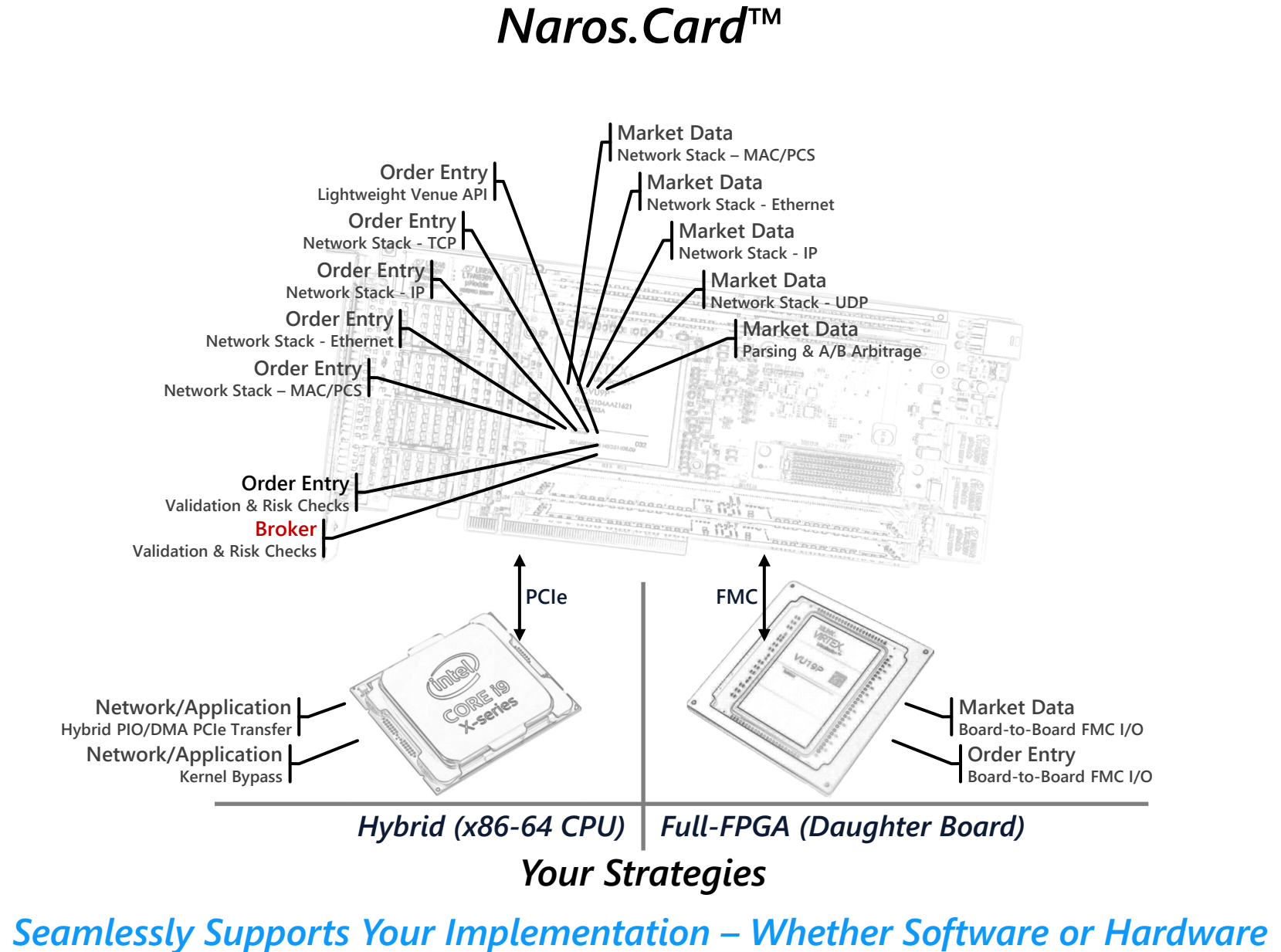
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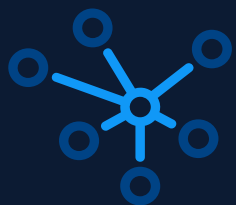
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Modularity
Brings...

*Flexibility
For Today & Tomorrow*












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Transforming
The
Trading
Stack...

*Captures Alpha
& Cuts OpEx
Incrementally Or
At Once*

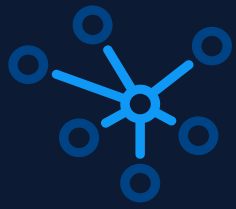
Trading Stack Investment Revisited

			Current Practice	Inventing the Future - Naros.Card™ ⁶	
			Software (x86-64)	Hybrid	Full FPGA
Trading Stack	Internal	 Trading Strategy Processing	CPU Cores Diverted	CPU Cores Reclaimed	CPU Dependency Ended
		 Trading Validation & Risk Checks	600ns to 1600ns	0ns ⁵	0ns ⁵
		 Kernel Bypass & PCIe & Network Stack	927ns <= 805Mbps ¹	899ns <= 1000Mbps ²	141ns <= 7500Mbps
		 Trading Market Data Parsing	800ns to 2200ns	36ns	36ns
		 Trading Exchange Communication	Native Protocol	Custom API ^{3a}	Custom API ^{3b}
	External	 Broker Validation & Risk Checks	350ns ^{4a} to 1200ns ^{4b}	0ns ⁵	0ns ⁵
		 OSI Layer 2/3/4 Expanded Functionality	800ns to 3600ns	0ns ⁵	0ns ⁵
Total Latency			3827ns to 9527ns	935ns	177ns

¹ Non-performant @ 810Mbps and above – insufficient to handle 60%+ of typical market data bursts ² 976ns <= 3000Mbps – sufficient to handle 99%+ of typical market data bursts ³ a) Reduces message size by 50%+ (depending on protocol) significantly improving PCIe transfer; b) PCIe transfer eliminated ⁴ As Claimed: a) Fusion Raptor; b) Fixnetix i-Execute ⁵ Conducted in-parallel with network stack functions resulting in zero practical/effective latency ⁶ US Patents 9,501,795, 10,269,071, 10,868,707, 10,880,211; Others Pending

Not STAC Benchmarks

Deploy Your Resources To Focus On Differentiating Competitive Advantages



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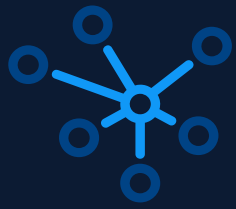
*It Does
What It Says
On The Tin*

LMS Is Committed To Transparency and Accuracy



Not a STAC Benchmark

At LMS We Create Real Solutions To Resolve Problems



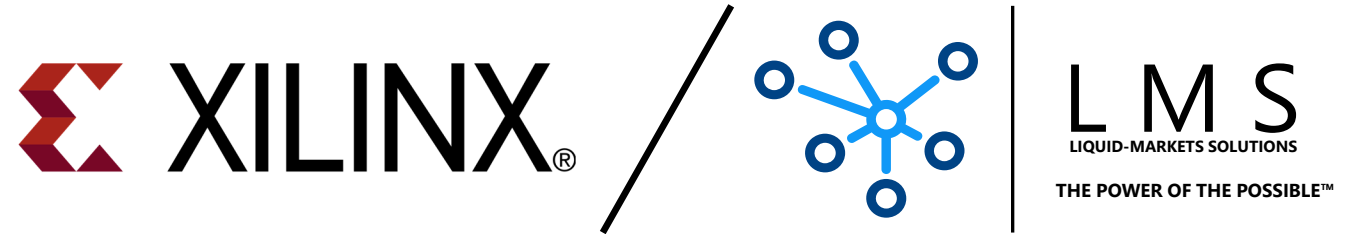
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TaSR™ - Complimentary Time-Limited Use

Xilinx & LMS...

*Are
Committed
To
Your
Success*



Use TaSR™ To Expose Bottlenecks & Identify Opportunities



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The Global Standard
Ultra-Low-Latency
&
Ultra-High-Capacity
Venue Access
&
Connectivity

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SG: +65-8515-8557