Ultra Low Latency Networking
with Algo-Logic on Intel PAC D5005 FPGA

May 2021

Algo-Logic Systems Inc.

- **Respected and trusted partner**
  - That develops innovative algorithms that run in FPGA logic

- **Customers include:**
  - Large Multinational Banks
  - Proprietary Trading Firms
  - Stock Exchanges

- **Algo-Logic provides FPGA solutions**
  - Tick-to-Trade systems with deep sub-microsecond latency
  - Pre-Trade Risk Checks for multiple worldwide exchanges
  - IP Cores for Ultra-Low-Latency (ULL) MAC, TCP, UDP, and associative lookup (EMSE)
  - Frameworks to trade on multiple exchanges

The Next Generation of Trading Systems

- **Execute Software on fastest CPU**
  - Intel Xeon Scalable Platinum processor
  - Just-released 11th generation Intel Core processor

- **New instructions for AVX-512**
  - Leverage new instruction to move 512 bits in one assembly instruction
  - Bypass operating system kernel using **Intel Data Mover**
  - Trade from software with round-trip under 1.5 microseconds*

- **Offload networking to FPGA**
  - Write your business logic in C/C++ with High Level Synthesis (HLS)
  - Process TCP orders in under 0.4 microseconds* in logic
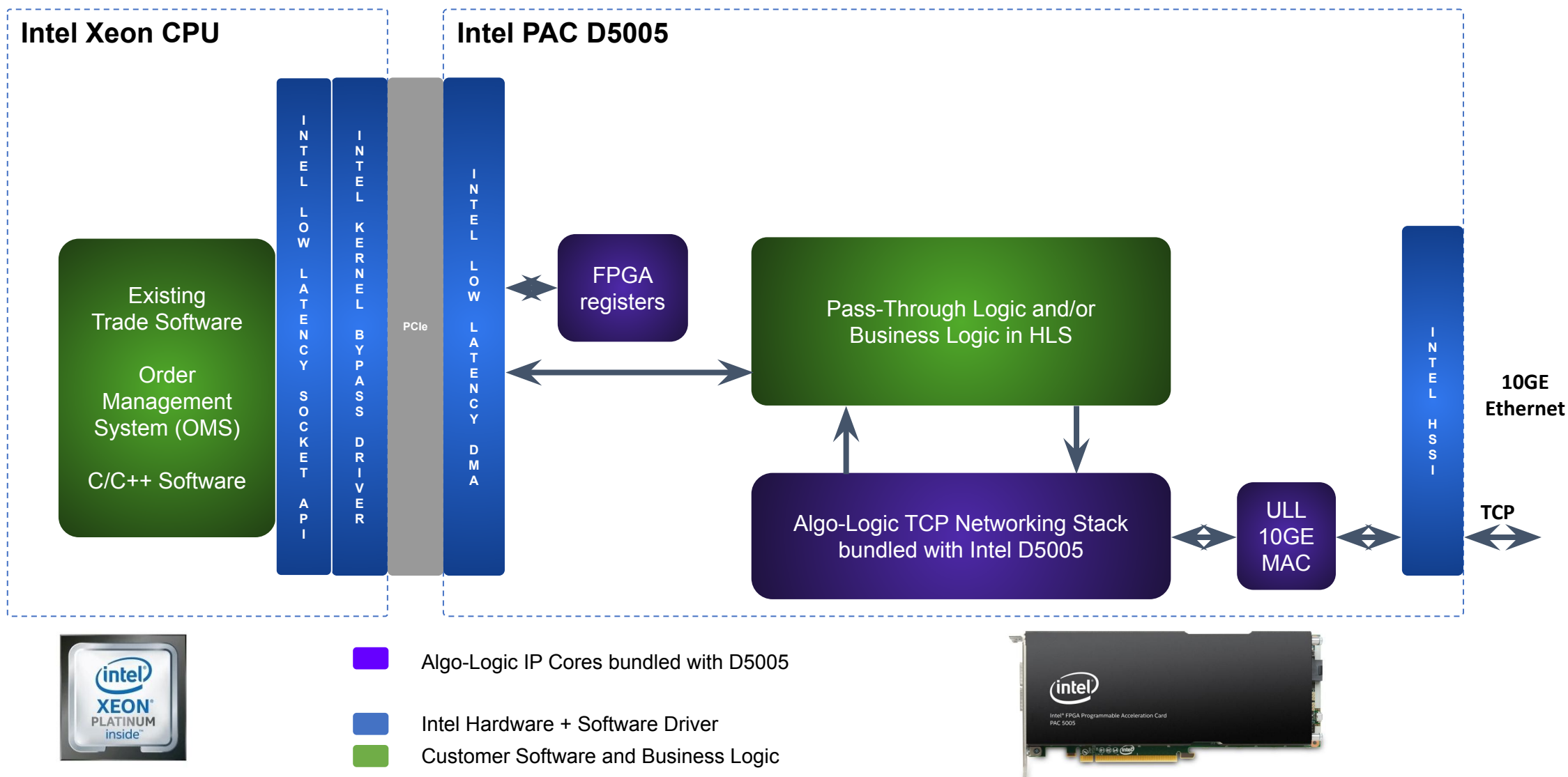 - Process market data in under 0.2 microseconds* using logic

Not a STAC Benchmark

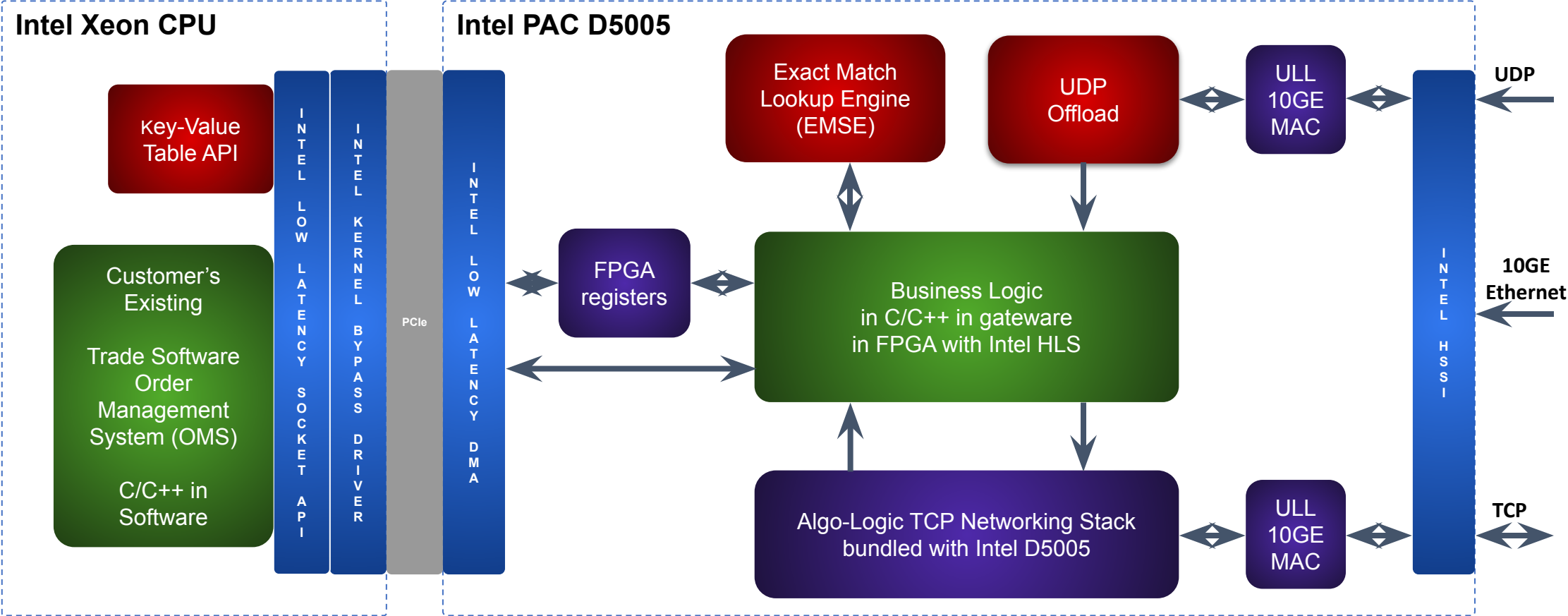# Crossing the Chasm from Software to Gateware

- **The Intel / Algo-Logic Advantage**
  - Framework enables success with FPGA
  - Accelerates existing Order Management Software
    - Enhances your OMS instead of replacing it
  - Algo-Logic's networking stack runs entirely in FPGA logic
    - Ultra-Low Latency Ethernet and TCP implemented entirely in FPGA
    - Enables logic on Intel PAC D5005 to trade faster than the best NICs

- **Easy Engagement Path**
  - No Verilog design skills required
    - Application logic written in C/C++ targets software and FPGA using HLS framework
  - Targets multiple exchanges
    - Use HLS to parse market data and send orders for execution

- **Rapid path to functional trading**
  - Measure time to your first trade in **weeks** not years

ALGO-LOGIC

Algo-Logic / Intel: Base ULL MAC + TCP + Data Mover Reference Design

Intel Xeon CPU

Intel PAC D5005

Existing Trade Software

Order Management System (OMS)

C/C++ Software

INTEL LOW LATENCY SOCKET API

INTEL KERNEL BYPASS DRIVER

PCIe

INTEL LOW LATENCY DMA

FPGA registers

Pass-Through Logic and/or Business Logic in HLS

Algo-Logic TCP Networking Stack bundled with Intel D5005

ULL 10GE MAC

INTEL HSSI

10GE Ethernet

TCP

Algo-Logic IP Cores bundled with D5005

Intel Hardware + Software Driver

Customer Software and Business Logic

Algo-Logic + Intel Extended Framework

Intel Xeon CPU

Intel PAC D5005

- Key-Value Table API
- Customer's Existing Trade Software Order Management System (OMS) C/C++ in Software
- INTEL LOW LATENCY SOCKET API
- INTEL KERNEL BYPASS DRIVER
- PCIe
- INTEL LOW LATENCY DMA
- FPGA registers
- Exact Match Lookup Engine (EMSE)
- UDP Offload
- ULL 10GE MAC
- Business Logic in C/C++ in gateware in FPGA with Intel HLS
- INTEL HSSI
- UDP
- 10GE Ethernet
- TCP
- Algo-Logic TCP Networking Stack bundled with Intel D5005
- ULL 10GE MAC

Legend:
- Algo-Logic IP Cores bundled with D5005
- Additional Algo-Logic IP Cores
- Intel Hardware + Software Driver
- Customer Software and Business Logic

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Solution for Ultra Low Latency Networking with FPGA
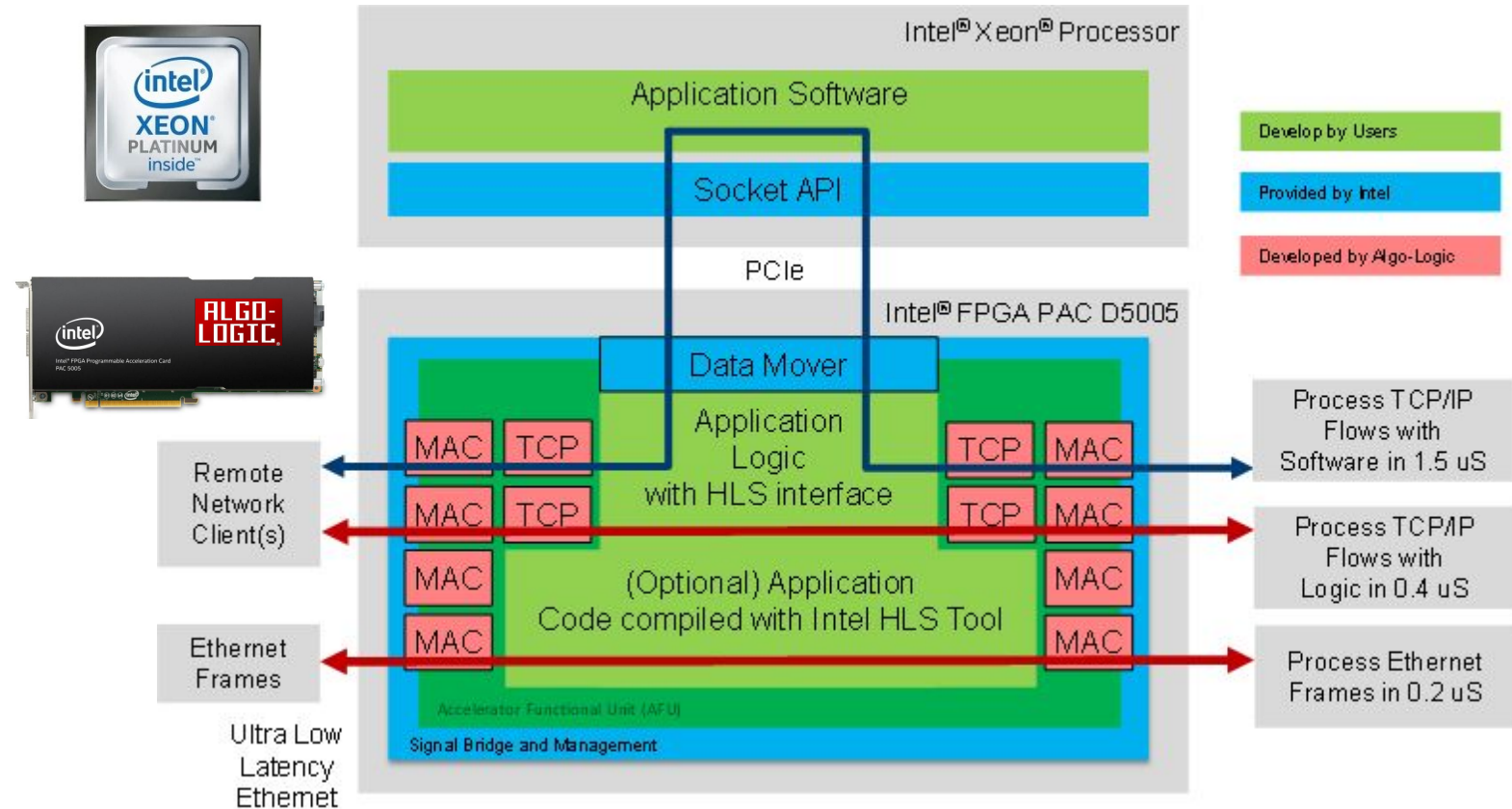
- **Intel PAC D5005 Platform**
  - PCIe card with Stratix 10 FPGA
  - Fast Data Mover to host CPU
  - High Level Synthesis (HLS)

- **Algo-Logic Provides**
  - Ultra-Low Latency MACs
  - TCP Endpoints in Logic
  - APIs for C/C++ software apps

- **Ideal Solution for**
  - High-speed Trading
  - Pre-Trade Risk Checks
  - Trading Gateways

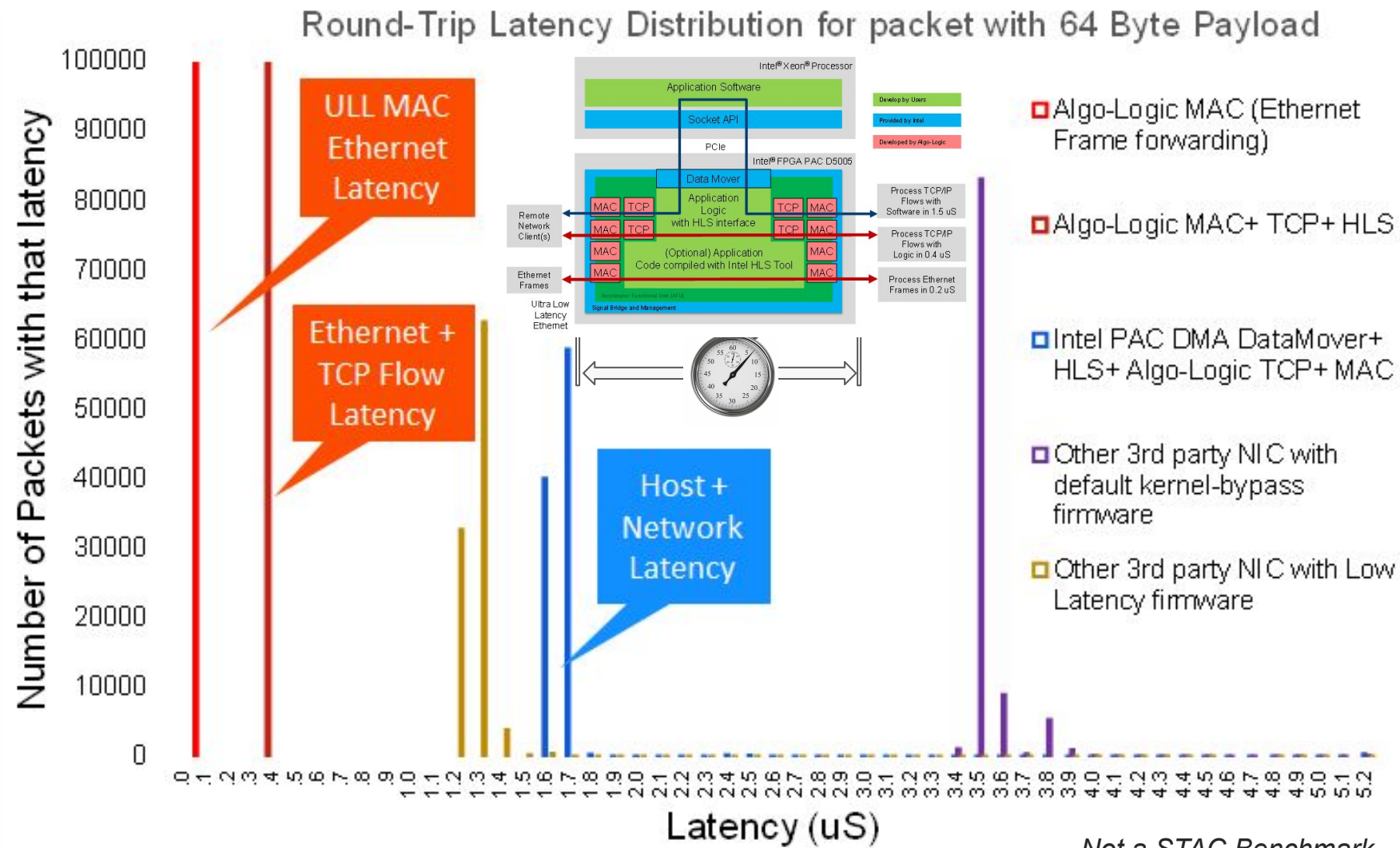# Round-Trip Application Latency

Other 3rd party NIC
- **Kernel Bypass**
- **Default Firmware**
- **Low Latency Firmware**

This Host+Network
- **Software API**
- **Intel Data Mover**
- **Algo-Logic MAC+TCP**

Algo-Logic FPGA Logic
- **ULL MAC**
- **TCP Endpoint**
- **HLS Interface for trading algorithms in logic**

Not a STAC Benchmark

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Conclusion

FPGA provide Ultra-Low Latency (ULL) Trading
- Run your existing OMS software on the fastest CPU
- Process market data and orders in nanoseconds with the FPGA
- Respond to the market instantly

[Algo-Logic/Intel D5005 Reference Design](#) **includes:**
- **Algo-Logic** ULL MAC in FPGA
- **Algo-Logic** TCP in FPGA
- **Intel** Data Mover **leverages new** AVX-512 instructions
- **Intel** High Level Synthesis **(HLS)** framework

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Algo-Logic's extended Tick-to-Trade platforms
- UDP for market data
- KVS for Associative Lookup
- **Support for markets including Nasdaq, ASX, CME, CBOE…**

To learn more, email us at: IntelSupport@algo-logic.com, tick to box on the **response card**,
and join the **fast data deeper dive** chat lounge