

# The FPGA Development Framework

Build your FPGA trading system in no time\*



# Why Enyx?

Our value lies in our expertise, with over a decade of experience building reliable solutions that get the job done.

Our goal is to not only be the best at developing complex information systems for finance, but also lead the way in promoting transparency through open testing and reporting.



[www.enyx.com/performance](http://www.enyx.com/performance)

# Our Products

## nxAccess Trade

An end-to-end market access solution that fully processes, filters and normalizes raw market data and can send orders both from a hardware and a software trading algorithm.

## nxFeed Distribute

A full-featured ultra-low latency market data distribution system, which utilizes the power of FPGA technology to offer wire-speed performance and jitter-free determinism.

## nxLink Connect

With fair bandwidth sharing and smart fiber arbitration, our wireless link management product suite is designed to build next generation, low latency trading infrastructure

## nxFramework Develop

Our industry-first development kit for financial institutions to build FPGA-enabled solutions in-house, including pre-trade risk checks, smart order routing, and trading platforms.

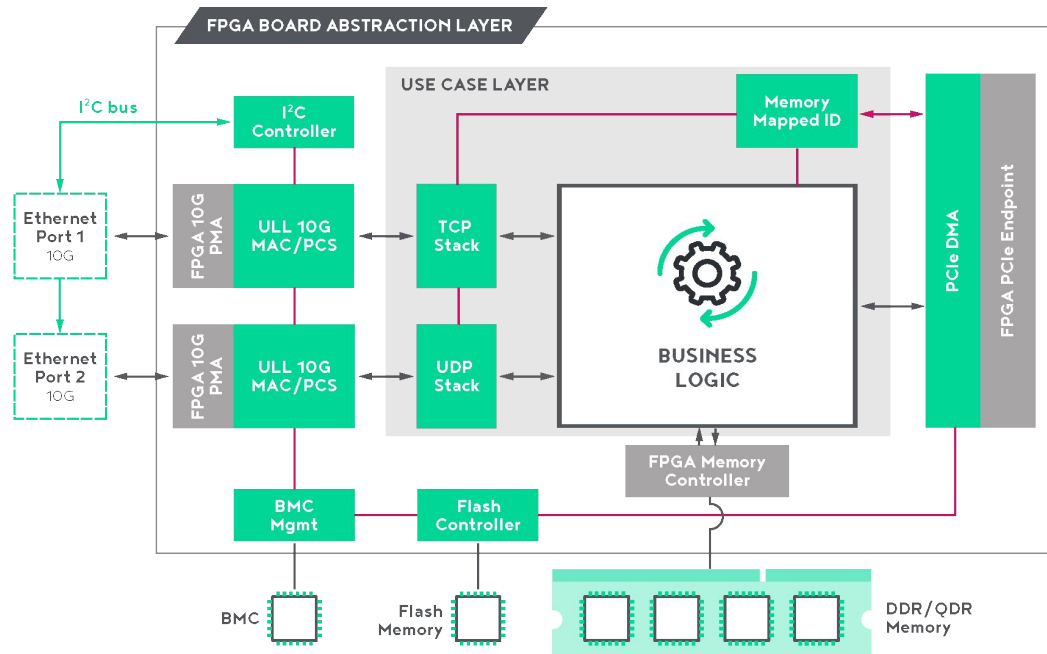
nxFramework

# The FPGA development framework for finance

- Hardware & software development environment for FPGA applications
- Based on 10 years of research & development
- Foundation for all Enyx off-the-shelf solutions
- **ULL IP Cores:**
  - 1G/10G MAC + PCS (37 ns RTT)\*
  - 1G/10G full TCP stack (82 ns RTT)\*
  - 1G/10G full UDP stack (76ns RTT)\*
  - PCIe streaming DMA (790ns RTT)\*
- **Additional features:**
  - Library of 60+ IP cores for MMIO, streaming manipulation, math functions, cache & memory management
  - A web-based GUI for configuration & debug
  - Linux drivers, communication & IP core management libraries
  - Off-the-shelf, configurable reference designs

nxFramework

# The FPGA development framework for finance





# What is included?

Board Support Package (BSP)

Xilinx Alveo, Bittware,  
Reflex CES, Arista 7130



# What is included?

Configuration Files + Build Workflow Scripts

YAML IO/frequency configuration  
Project workflow Python scripts

Board Support Package (BSP)

Xilinx Alveo, Bittware,  
Reflex CES, Arista 7130



# What is included?

## Core Hardware IPs + Software Libraries

MAC/PCS, TCP, UDP, PCIe DMA  
C++ libraries & Linux drivers

## Configuration Files + Build Workflow Scripts

YAML IO/frequency configuration  
Project workflow Python scripts

## Board Support Package (BSP)

Xilinx Alveo, Bittware,  
Reflex CES, Arista 7130



# What is included?

**NEW****Hardware MM & IO IP Libraries**

**Streaming bus manipulation**  
**Memory Mapped & math functions**

**Core Hardware IPs + Software Libraries**

**MAC/PCS, TCP, UDP, PCIe DMA**  
**C++ libraries & Linux drivers**

**Configuration Files + Build Workflow Scripts**

**YAML IO/frequency configuration**  
**Project workflow Python scripts**

**Board Support Package (BSP)**

**Xilinx Alveo, Bittware,**  
**Reflex CES, Arista 7130**

# What is included?

**NEW**  
**Market  
Data  
IPs**

**NEW**  
**Order  
Execution  
IPs**

**NEW**  
**Bandwidth  
Management  
IPs**

Market data decoders  
Order & book management  
Execution stack  
Bandwidth management

**NEW**  
**Hardware MM & IO IP Libraries**

Streaming bus manipulation  
Memory Mapped & math functions

**Core Hardware IPs + Software Libraries**

MAC/PCS, TCP, UDP, PCIe DMA  
C++ libraries & Linux drivers

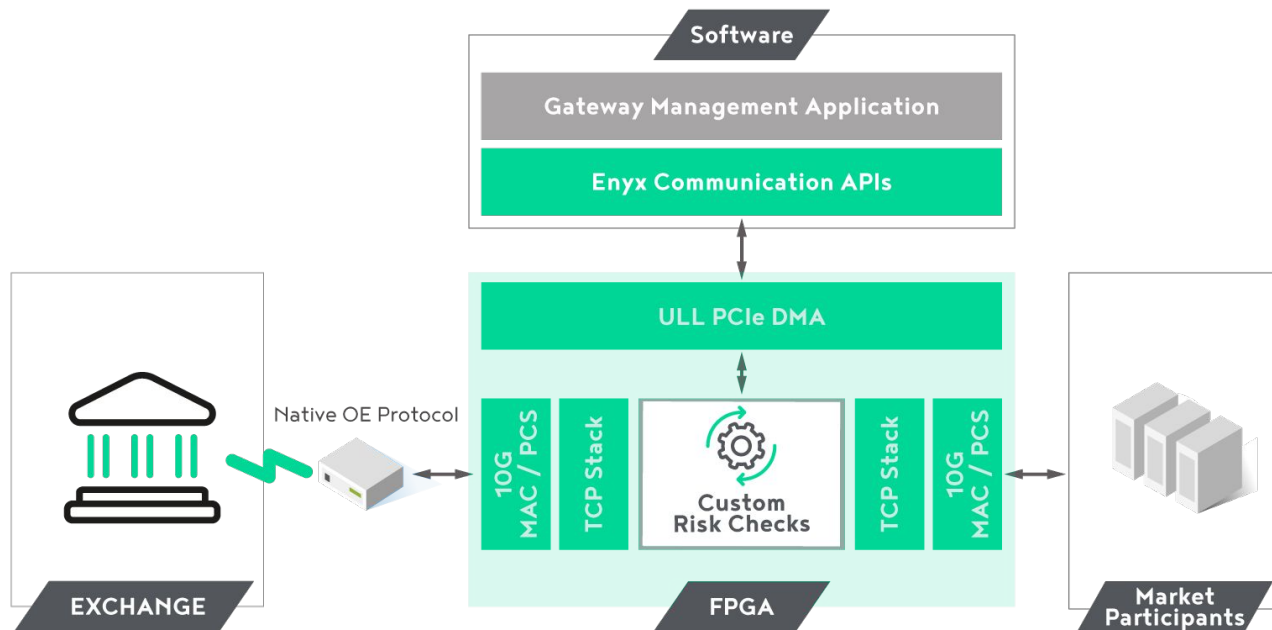
**Configuration Files + Build Workflow Scripts**

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# Use case: Risk check gateway

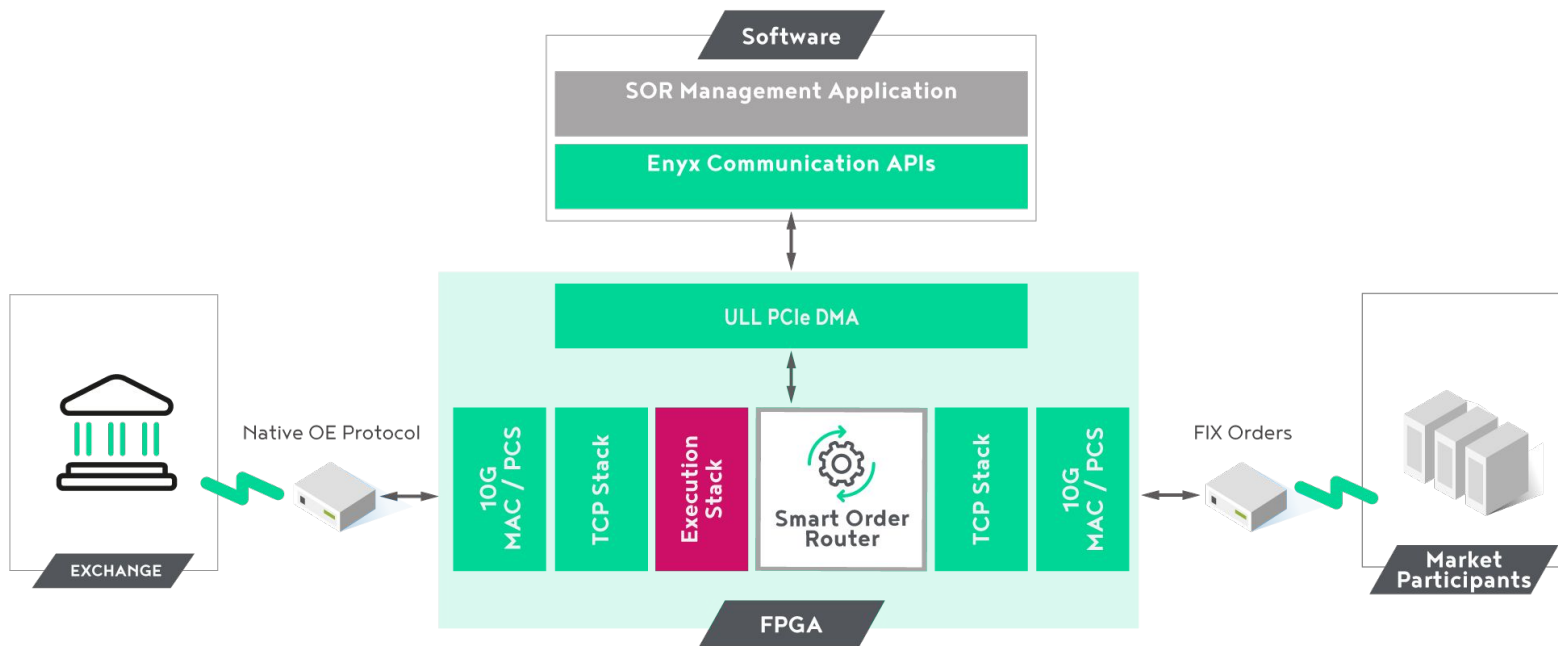


- ✓ 10G MAC + PCS
- ✓ 10G full TCP stack
- ✓ PCIe streaming DMA

- ✓ PCIe MM register management
- ✓ Linux drivers & C++ libraries
- ✓ Synthesis to bitstream workflow

- ✓ Hardware IP Libraries:  
(ST/MM/Math/Memory/Cache)

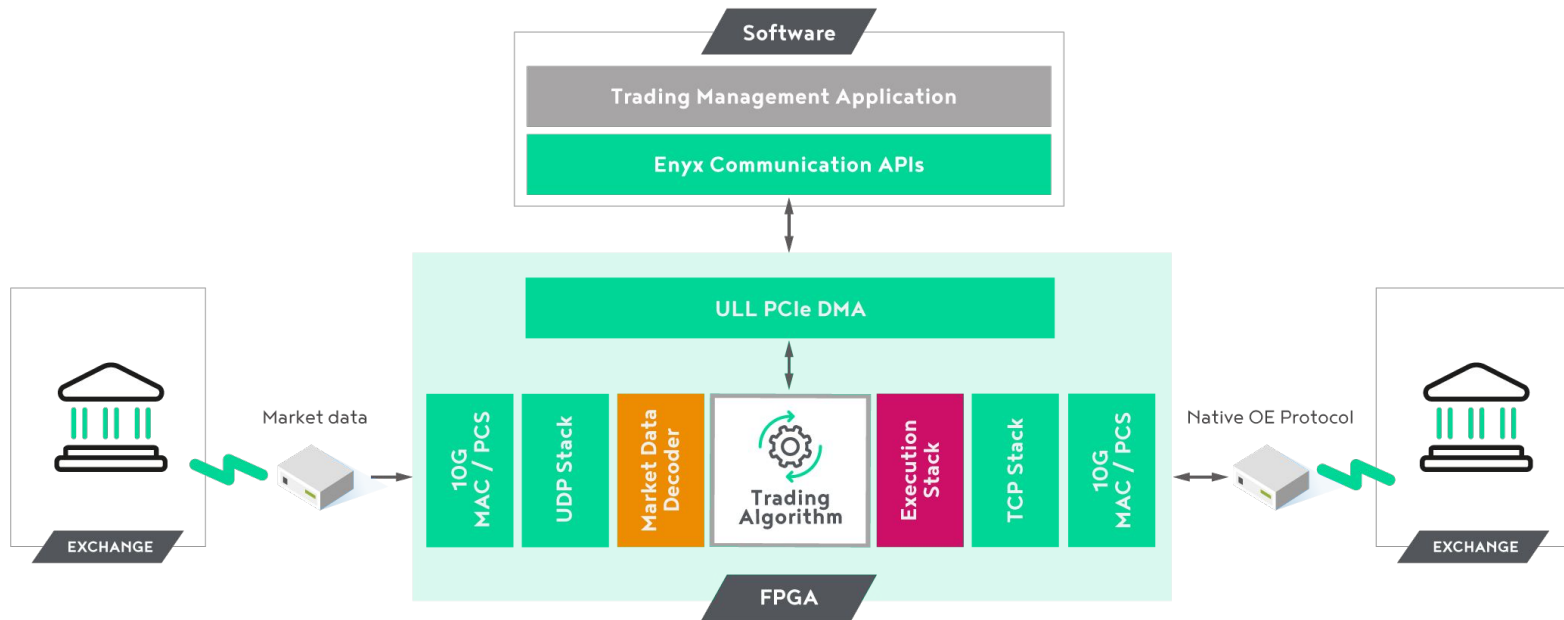
# Use case: Smart Order Router



- ✓ 10G MAC + PCS
- ✓ 10G full TCP stack
- ✓ PCIe streaming DMA

- ✓ PCIe MM register management
- ✓ Linux drivers & C++ libraries
- ✓ Synthesis to bitstream workflow
- ✓ Hardware IP Libraries: (ST/MM/Math/Memory/Cache)
- ✓ Execution gateway

# Use case: ULL tick-to-trade

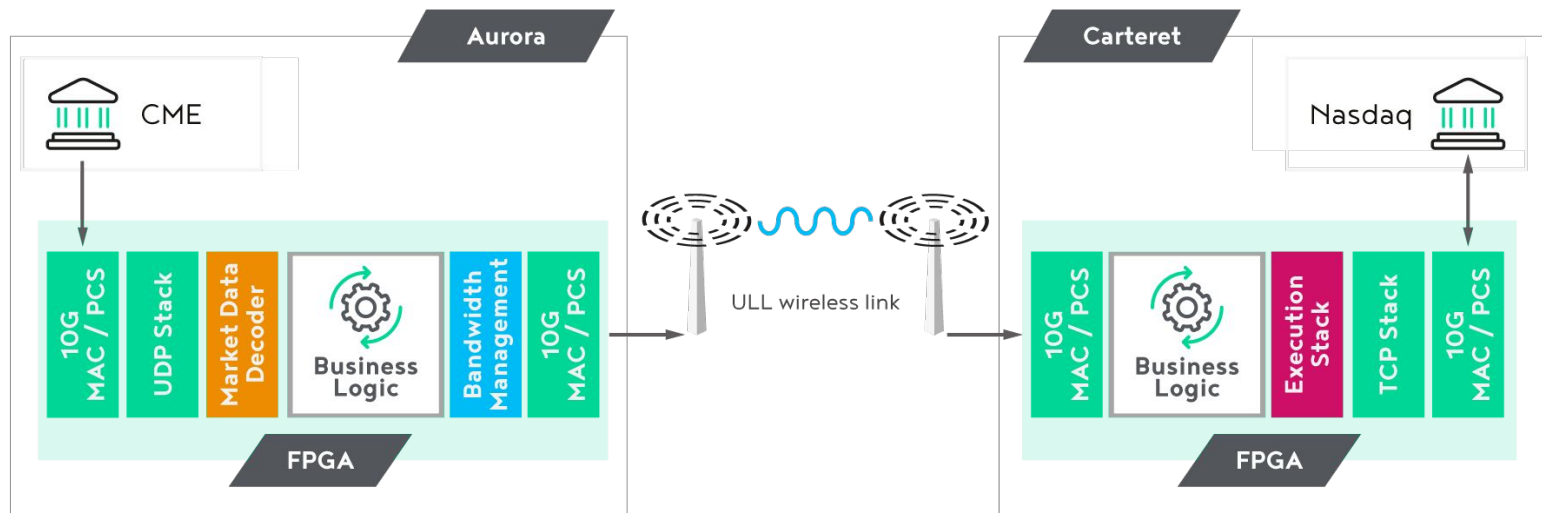


- ✓ 10G MAC + PCS
- ✓ 10G full TCP stack
- ✓ 10G UDP stack
- ✓ PCIe streaming DMA

- ✓ PCIe MM register management
- ✓ Linux drivers & C++ libraries
- ✓ Synthesis to bitstream workflow
- ✓ Hardware IP Libraries:  
(ST/MM/Math/Memory/Cache)

- ✓ Execution gateway
- ✓ Market data decoder(s)

# Use case: Signal over wireless

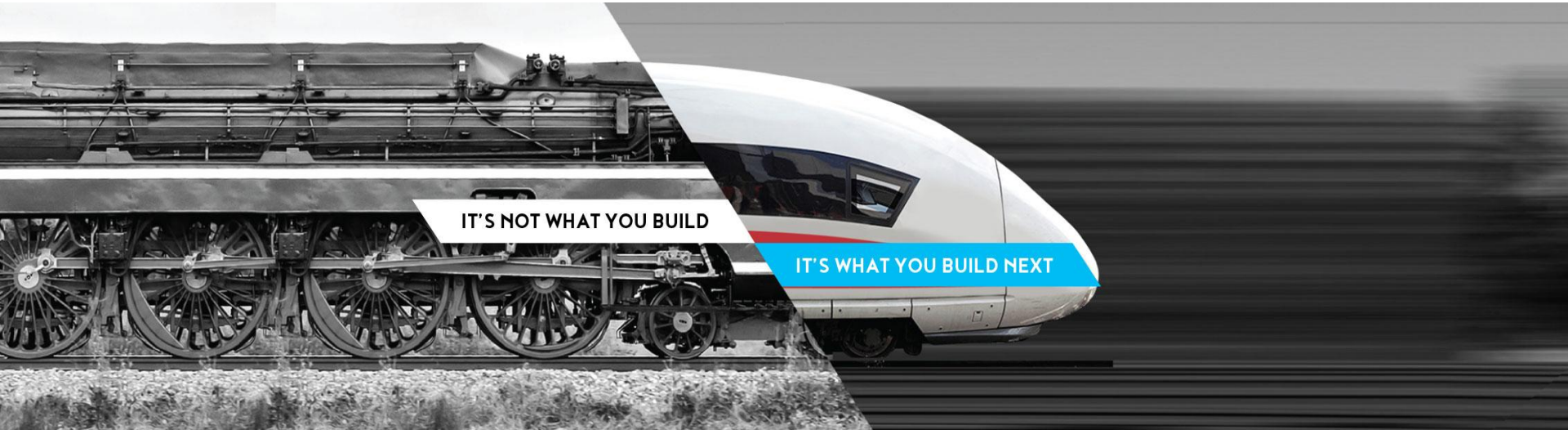


- ✓ 10G MAC + PCS
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- ✓ PCIe MM register management
- ✓ Linux drivers & C++ libraries
- ✓ Synthesis to bitstream workflow
- ✓ Hardware IP Libraries:  
(ST/MM/Math/Memory/Cache)
- ✓ Execution gateway
- ✓ Market data decoder(s)
- ✓ Bandwidth management

# Thank you!

Check the Enyx box for more information



To access our downloadable material: <http://info.enyx.com/global-stac-live20>

