STAC™ BENCHMARK COUNCIL

STAC® Performance Summit

June 22, 2011
Doors open at 1:00pm
Meeting starts at 1:30pm
Meeting will be followed by cocktails

Hotel Monaco
225 North Wabash Avenue
Paris Room
Chicago

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JUNIPER NETWORKS

Mellanox TECHNOLOGIES

Panel Discussion: The State of Hardware Acceleration

Off-loading the processing of network and trading-venue protocols to programmable hardware was once fringe and is now an accepted pattern. Where is it headed? How are hardware-oriented solution vendors continuing to add value? What are the roadmaps like for underlying components such as FPGA? Is I/O the only domain amenable to a hardware-based approach? What about trading algorithms? Leading vendors will make short presentations related to their offerings, then sit together to address these topics and questions from attendees.

Mike Mayhew, Product Manager, TTNET, Trading Technologies, Inc. (moderator). Mike has over 15 years experience designing hardware systems for defense, tele-comms and HFT applications. Specializing in embedded microprocessor subsystems and high-speed digital communications, he has design experience with a range of technologies including communication processors, network processors, Field Programmable Gate Arrays (FPGAs) and other programmable logic. Prior to joining Trading Technologies, Mike held design positions at ITT Aerospace, Tellabs and a California-based start-up, Turin Networks (now Force10 Networks). Before taking on product management of Trading Technologies' global hosting environment, he was responsible for initiating a project that ported proprietary messaging software to hardware. Mike holds a Bachelor of Science in Electrical Engineering from Valparaiso University and an MBA in Strategy and Finance from the University of Chicago.

David Taylor, VP Product Architecture, Exegy. **[slides]** David is responsible for the definition, architecture, and delivery of Exegy's high-performance computing appliances for the financial services market. Previously as VP of Engineering, David led a talented group of experienced software, hardware, and verification engineers, as well as financial market data business analysts and feed handler developers. As an architect and engineer, he has developed numerous patent-pending algorithms and architectures that provide Exegy products with industry-leading performance, functionality, scalability, and reliability. Prior to joining Exegy, David was a Visiting Assistant Professor in the Department of Computer Science and Engineering and was actively involved in computer communications research at the Applied Research Laboratory at Washington University in Saint Louis.

Mark Skalabrin, Founder and CEO, Redline Trading Solutions. [slides] Mark is a 20-year veteran of the high-performance computing industry. Throughout his career, Mark has built engineering-centered businesses that combine leading-edge technology with application acceleration expertise to solve some of the most challenging computing problems across multiple markets. Before he founded Redline, Mark served eight years as General Manager and Corporate Officer at Mercury Computer Systems. He holds a BS degree in Electrical and Computer Engineering from Washington State University.

Olivier Baetz, VP Sales and Operations, North America, NovaSparks. **[slides]** Olivier joined NovaSparks in April 2011, bringing over ten years of experience selling and implement-ing low latency technology solutions for the financial industry. In 2000, Olivier was part of the original team at Radianz, the first global Extranet for the financial industry. At Radianz, Olivier successfully designed the solution for the original "proof of concept" customer which established the value of the Radianz community model. He also ran the North American Sales Engineering team for five years and was instrumental in the creation of the Radianz ULTRA service which provides ultra-low latency exchange con-nectivity to high-frequency trading firms. In 2009 and 2010, Olivier built and led the glo-bal technical convergence project team to integrate the Radianz platform into the global BT Network. Olivier started his career in telecoms designing and selling managed net-work solutions for large multinational firms. Olivier holds a MS in Telecom Engineering from ENST Paris and an MBA from Wharton with a major in Finance. When he is not working, Olivier enjoys sailing, surfing, skiing and all good wines from around the world.

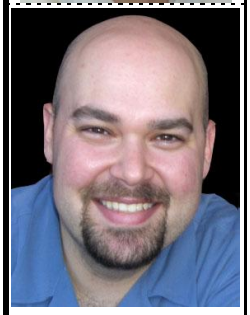
Innovation Roundup – Round 1

• "Solarflare: The platform for precision timing" **[slides]**	**Bruce Tolley,** VP of Solutions Marketing, Solarflare
• "Low Latency 10Gb Ethernet With Chelsio WireDirect™" **[slides]**	**Troy Leedberg,** Sales Manager, Chelsio
• "When ultra-low latency is not fast enough: Monitoring at the speed of trading" **[slides]**	**Buck Bundhund**, VP of Sales, NetOptics

Navigating Low-Latency Network Choices

If one word could summarize what trading organizations face when it comes to low-latency networking, it would be "choice." Choice of transport (Infiniband and Ethernet of various speeds). Choice of API (sockets, RDMA/verbs, and more). Choice of implementation (increasing variety of switch and NIC vendors focused on low latency). What should customers consider when making these choices? How do the solutions differ? Put your questions to some innovative vendors, who will make short presentations then sit together for a Q&A moderated by Chicago HFT veteran.

Tony Verga, CEO, HFT Technologies LLC (*moderator*). HFT Technologies is a leading provider of high frequency trading consulting and technology for the financial community that specializes in high-speed infrastructures and trading application development for algorithmic trading and market making. For the past 15 years, HFT Technologies' founding partners have helped some of the industry's biggest players with high speed exchange connectivity, LAN/WAN design, proximity co-location, algorithmic trading application design and engineering. HFT Technologies has extensive experience with all major global financial exchanges and all major protocols. Prior to HFT Technologies, Tony was the Director of Infrastructure for some of Chicago's largest prop shops and also held the position of Director of Technology for the NADEX exchange.



Jeff Margolis, Solutions Architect, Mellanox Technologies. **[slides]** Jeff works with financial services organizations to implement low latency networking solutions for high frequency trading. In this role, he deploys Mellanox solutions at a large array of investment banks, hedge funds and exchanges. Prior to Mellanox, Jeff spent more than three years as the central region FSI Systems Engineer at Voltaire, where he was responsible for designing and implementing large trading platforms based on InfiniBand and 10GbE. Before joining Voltaire, Jeff held a variety of network, systems and support engineering positions at The Revere Group, Interwoven and Sprint. Jeff holds a BA in Telecommunications from Michigan State University.

John Moore, Director, Financial Services Marketing, Juniper Networks. **[slides]** John sets strategy and direction for Juniper's message to Banks, Exchanges and Investment houses around in all theaters. In this role, John drives feature roadmaps, solutions development and field readiness to make sure that Financial customers have the products, solutions and services to use Juniper products for competitive advantage. John brings two decades of experience working with the financial sector in a career spanning Sun Microsystems, Cisco and Juniper Networks.

Dean Nebrig, Director of Central Region Sales, Arista Networks. **[slides]** Dean joined Arista in December of 2009 after 5 years with Thomson Reuters in the Market Data Business Unit. For over 25 years, Dean has been engaged in the networking and financial data industry with both established companies like Cisco Systems and Sprint but also with startup ventures. With Arista, Dean has worked extensively with the financial industry in Chicago in establishing Arista as a prominent supplier of low latency solutions to the HFT and Proprietary trading community.

COFFEE BREAK

STAC Update

Peter will review benchmark and tools activity in a number of the STAC Benchmark domains, including feed handlers, gateways, messaging middleware, tick databases, and risk management.

Peter Lankford, Founder & Director, Securities Technology Analysis Center. **[slides]** Peter has overseen STAC since its birth in 2006. Before that, Peter was SVP of Information Management Solutions at Reuters, where he led the $240M market data systems business. Peter's team led Reuters into the business of low-latency direct feeds and catalyzed the widespread adoption of Linux on Wall Street by making RMDS available on that platform. Prior to Reuters, Peter held management positions at Citibank, First Chicago Corp., and operating-system maker IGC. Peter has an MBA, Masters in International Relations, and Bachelors in Chemistry from the University of Chicago.

Innovation Roundup – Round 2

• "TIBCO FTL 1.1 - An overview of TIBCO's STAC-M2 Numbers" **[slides]**	**William McLane**, Product Architect TIBCO Messaging, TIBCO
• "Avoiding Post Trade Pitfalls – Increasing Simplicity, Capacity and Transparency" **[slides]**	**Bill Romano**, Senior Systems Engineer, Solace Systems
• "How to detect and fix hard-to-find concurrency errors in multi-threaded systems" **[slides]**	**Eric Scollard**, VP of Sales and Services, Corensic

Optimizing x86 Apps

Trading applications—whether written in C/C++, Java, or other languages—regularly need their latency reduced, their capacity increased, or both. But not all x86 apps take full advantage of the platform, and the gap can widen with time as platforms add features and as cores per server increase. What are the best practices for design, development, and testing of applications? What are the best choices of language, threading models, tools, and compilers? An expert panel will tackle these issues and your questions.

Michael D'Mello, Program Manager, Tools Immersion Program, Intel. Under Michael's leadership, the Tools Immersion Program program has provided Intel Software Tools based solutions to some of the most challenging software performance problems encountered in industry. Prior to his current role at Intel, Michael held various senior technical positions at the Hewlett-Packard Company, Convex Computer Corporation, and Thinking Machines Corporation. Michael has over 20 years of experience in the parallel computing industry. He holds a Ph.D. in Chemical Physics from the University of Texas at Austin.

Stephane Raynaud, Lead Principal Engineer, RogueWave Software. Stephane's responsibilities include extensive work in the financial services markets in New York, Boston and Toronto as well as supporting architects in a broad range of systems from Quantitative Analysis to low-latency systems. Most recently Stephane has been focusing on how to better address CPU Cache optimization for multi-core processors. Originally from France, Stephane emigrated to North America in the early 1990's. In the years since, Stephane has become a skilled developer as well as an accomplished leader. By heading large-scale software development and consulting projects, Stephane has developed extensive expertise in software architecture.

Peter Godman, Founder & CEO, Corensic. Peter joined Corensic from Isilon Sytems where, as Director of Software Engineering, he led development of several major releases of Isilon's award-winning OneFS distributed filesystem and developed around twenty patent-pending technologies. Prior to his six year tenure at Isilon, Peter led development of several generations of Linux-based client software at RealNetworks.