STAC BENCHMARK COUNCIL™

STAC® Summit

November 4, 2013
Doors open: 9:30am
Meeting starts: 10:00am

Illinois Institute of Technology
Auditorium
565 W Adams Street
Chicago, IL 60661

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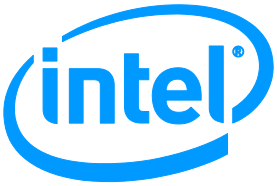

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AGENDA

BIG WORKLOADS

STAC Update – Big Workloads [slides]

- *Peter Lankford, Founder & Director, STAC*

STAC will review progress on Council activities related to workloads involving big data and big compute.

Parallel File Systems

- *Doris Conti, Director, Cross Systems Software including GPFS, IBM* [slides]
- *Dan Ferber, Sr Manager, Systems Engineering, Intel* [slides]
- *Glenn Wright, Systems Architect, DataDirect Networks* [slides]

Parallel file systems are starting to get significant attention on Wall Street, and it's no surprise. Whether searching for alpha or quantifying risk, each trading firm has more and more compute nodes trying to access large data stores simultaneously. Data bottlenecks are rife. Parallel file systems--many of which hail from supercomputing or the web-scale industry--seem to promise great acceleration for data-intensive analytics. A panel of experts will offer their views.

Innovation Roundup – Round 1

"Scalable Informatics Time Series Analytics appliance" [slides]	*Joe Landman, Founder and CEO, Scalable Informatics*
"Driving big workloads with the world's fastest all flash, scale-out SAN: The Kaminario K2" [slides]	*Bill Bodei, Senior Director, Kaminario*
"RDMA for the Masses" [slides]	*Kurt Rago, Sr. Systems Engineer, Mellanox Technologies*
"Vertically Scaling Messaging Systems to Meet the Needs of Big Data" [slides]	*Bill Romano, Sr. Systems Engineer, Solace Systems*
"Next generation technologies for virtualized workloads: An Overview of the Solarflare SFN7122F 10/40GbE Server Adapter" [slides]	*Bruce Tolley, Vice President of Marketing, Solarflare Communications*

Technical Brief: OpenCL for FPGA

- *Ken Hill, Researcher, CHREC* [slides]

The National Science Foundation (NSF) Center for High-Performance Reconfigurable Computing (CHREC, pronounced "shreck") is a national research center and consortium of more than 30 industry, government, and academic partners working collaboratively to solve research challenges at the nexus of reconfigurable, high-performance, and embedded computing. One of these challenges is making heterogeneous hardware accessible to mainstream developers via easy-to-use frameworks. In this talk, Ken will discuss one such framework: OpenCL. Ken will explain the OpenCL concept and how it works with FPGAs, then share some of CHREC's experiences with OpenCL on FPGAs in areas such as financial risk analysis.

Networking Luncheon

FAST WORKLOADS

STAC Update – Fast Workloads [slides]

- *Peter Lankford, Founder & Director, STAC*

STAC will review progress on Council activities related to low-latency, high-volume realtime workloads

Frontiers in Public and Private Markets

- *Shawn Sloves, Founder & Partner, Atlas ATS* [slides]
- *Wolfgang Eholzer, Head of Trading IT, Eurex Frankfurt AG* [slides]

While many of the major exchanges are focused on consolidation, another trend is quietly at work: exchanges are exploiting technology to open up new markets and transform existing ones. Whether in mature asset classes like futures, or instruments that are new to exchange trading like swaps and digital currencies, innovation continues to flourish. There are even cloud technology vendors offering to spin up a new exchange or dark pool in hours ("just add liquidity"). We'll ask some of the pioneers at the forefront of these trends how they are innovating, how they are exploiting technology, and what this means for the future.

Innovation Roundup – Round 2

"New Enhancements in Precision Time, Instrumentation, and Packet Capture with the Solarflare SFN7322F IEEE 1588 Precision Time Server Adapter" [slides]	*Bruce Tolley, Vice President of Marketing, Solarflare Communications*
"Building highest density networks at lowest latency" [slides]	*Anant Shah, Nexus Product Manager, Cisco*
"Shaving nanoseconds: pushing the frontiers of low latency networking" [slides]	*Matthew Chapman, CTO, Exablaze*

Technical Brief: The next stage in high-performance networking

- *Paul Grun, Vice Chair, OpenFabrics Alliance* [slides]

The world is adopting new ways to analyze avalanches of data. The data may be stored and accessed in new ways, such as from public and private clouds. And larger, complex problems are demanding new ways to collaborate. The OpenFabrics Alliance (OFA) believes that these trends demand new approaches to high-performance networking. For the past several years, the OFA has led the development of open source software for high- performance, low-latency communication in trading and scientific applications, via technologies such as RDMA. Now the OFA has begun an effort to drive high-performance networks to the next level in scope and performance. By focusing first on application requirements, the OFA intends to bring HPC-style benefits to new use cases. Paul will describe this approach and suggest ways that developers from the financial services sector can get involved in defining this next push forward in network technology.

Coffee Break

Technical Brief: Getting the most from Haswell

- *Arch Robison, Senior Principal Engineer, Intel* **[slides]**

The first of Intel's Haswell processors has been released to the market, with more on the way. This architecture supports new intrinsics and the Haswell New Instructions, which have the potential to reduce latency and accelerate compute- and data-intensive workloads. Arch will provide insight into the most promising of these innovations and where developers should focus their initial efforts.

Innovation Roundup – Round 3

"Embracing Open Source in the Enterprise" [slides]	*Scott Lasica, VP, Global Alliances, Rogue Wave Software*
"TIBCO FTL: Still the Fastest and now the Broadest" [slides]	*Bill McLane, Director Product Architecture, Messaging, TIBCO*
"CIARA ORION HF: The World's Fastest High-Frequency/Low Latency Servers" [slides]	*Jeff Cachat, Director of Business Development, Ciara Technologies*
"Latency Monitoring Solutions for Financial Trading Markets" [slides]	*Jerry Eschweiler, Regional Sales Director, Apcon*

Hardware acceleration today

- *Nikolaj Hermann, CTO, Fiberblaze* **[slides]**
- *John Lockwood, CEO, Algo-Logic* **[slides]**
- *Sanjay Shah, CTO, Nanospeed Technologies* **[slides]**

Seven years after the first well-known use of FPGA to accelerate financial workloads, what is the state of the art? Where does FPGA play in the trading process? What is the division of labor between vendors and internal staff? Where can we expect the technology to head? And hey: with all the talk of the latency race being "over", why are we still talking about FPGA?

Networking Reception

Speaker Biographies

Doris Conti, Director in Systems and Technology Group, Cross Systems SW including GPFS, IBM. Doris currently works for IBM as a software development director in Systems and Technology Group, She has responsibility for GPFS and HPC software. Prior to this role, Doris has held various other positions in IBM, including development, performance, product management, and marketing. She has worked on various software and hardware products, including the mainframe. Doris has a BS and MS degree in Computer Science. She lives in Poughkeepsie with her husband and three kids.

Wolfgang Eholzer, Head of Trading IT, Eurex Frankfort AG. Wolfgang is Head of Trading IT and in charge of the System Design for the Eurex trading system T7 as well as for the cash market trading system Xetra. Since 2007 Wolfgang has been in charge of the Eurex Technology Roadmap which resulted in the delivery of the high speed trading interfaces for order handling and market data. In addition, he is responsible for performance monitoring and capacity planning as well as for the implementation T7 the new trading system Eurex has recently launched. He is also in charge of new trading functionality and has a particular focus on achieving low latency and high throughput. Prior to his work for Eurex, Wolfgang was in charge of application development for the electronic trading systems Eurex and Xetra at Deutsche Börse Systems the IT subsidiary of Deutsche Börse Group. Before joining Deutsche Börse Systems, Wolfgang spent 2 1/2 years with Cambridge University, U.K., as a research associate in Applied Mathematics and Theoretical Physics.

Dan Ferber, Sr Manager, Systems Engineering, Intel. Dan leads the Systems and Solutions Engineering team for Lustre* at Intel. He is responsible for supporting Intel's Lustre community partners and customers in HPC and moving Lustre into Exascale. Dan previously ran Business Development and Strategic Partnerships at Whamcloud, a Lustre start-up acquired by Intel in July. Prior to Intel and Whamcloud, Dan had more than 20 years of high tech experience developing and supporting HPC communications software, configuration management tools, database software, I/O libraries and commercial software at Cray, SGI, Sun, and Oracle. He also managed engineering, support, and business development teams. Dan holds a Master's degree in Computer Systems from the University of St. Thomas in St. Paul, Minnesota, a Bachelor's degree from Occidental College in Los Angeles, and attended Phillips Exeter Academy in Exeter, New Hampshire. He has lived a year each in London, England and Barcelona, Spain and is permanently based in Minnesota. Dan's focus in on meeting customers' needs.

Paul Grun, Senior Technologist, Storage and Data Management, Cray. Paul's current focus at Cray is on large scale storage systems and system-level networking. During nearly 35 years, Paul has been engaged in all aspects of server I/O, ranging from hardware design of early generation RAID controllers to architecture and design of industry standard high performance networks to server chipset architecture. He was a key contributor to the creation of the InfiniBand Architecture and was responsible for creating the InfiniBand transport protocol. He also proposed a new approach to networking over Ethernet known as "RoCE" (RDMA over Converged Ethernet), chairing the working group charged with creating the RoCE specification and serving as its principle author. He is a past chair of the InfiniBand Trade Association's (IBTA) Technical Working Group and currently serves as a Director of the IBTA. He was recently appointed Vice Chair of the OpenFabrics Alliance, an industry organization dedicated to providing open source software stacks for high performance RDMA networks. As an Intel Principal Engineer, Paul oversaw a chipset architecture team charged with developing high end chipsets for servers and workstations. He holds four patents related to the application of RDMA technology to RAID system design and PCI.

Nikolaj Hermann, CTO, Fiberblaze. Nikolaj has been in charge of the development of the complete product portfolio at Fiberblaze, including all 10 GigE FPGA based Network Interface Cards. The network interface cards are now being used as the state-of-the-art choice at many High Frequency Trading sites worldwide. Before Nikolaj founded Fiberblaze in 2008, he worked in the electronics and telecommunication industry for more than 10 years and holds a degree in physics.

Kenneth Hill, NSF CHREC Research Assistant at University of Florida. Kenneth received his B.S. degree in Computer Engineering in 2011, and M.S. degree in Electrical and Computer Engineering in 2012 from the University of Florida, Gainesville. He is currently pursuing his Ph.D. in Electrical and Computer Engineering from the University of Florida and is a researcher in the NSF Center for High-Performance Reconfigurable Computing (CHREC). Ken's research interests include FPGA-based reconfigurable computing, heterogeneous systems, high-level synthesis tools for parallel computing, and parallel computing architectures. In particular, he is focusing on exploring the challenges of applying reconfigurable architectures to accelerate impactful applications in computational sciences.

Peter Lankford, Founder & Director, Securities Technology Analysis Center. Peter has overseen STAC since its birth in 2006. Before that, Peter was SVP of Information Management Solutions at Reuters, where he led the $240M market data systems business. Peter's team led Reuters into the business of low-latency direct feeds and catalyzed the widespread adoption of Linux on Wall Street by making RMDS available on that platform. Prior to Reuters, Peter held management positions at Citibank, First Chicago Corp., and operating-system maker IGC. Peter has an MBA, Masters in International Relations, and Bachelors in Chemistry from the University of Chicago.

John Lockwood, CEO, Algo-Logic. John is the founder and CEO at Algo-Logic Systems. Algo-Logic's hardware-accelerated logic circuits enable networks to achieve ultra-low latency processing while carrying large volumes of data. From 2006 to 2009, John managed the NetFPGA program as a Consulting Associate Professor at Stanford University. At Stanford, John grew the worldwide deployment of NetFPGA hardware from 10 to 1,021 units. Prior to joining Stanford in January of 2007, John led the Reconfigurable Network Group, which was a part of the Applied Research Laboratory at Washington University in Saint Louis. There he was a tenured Associate Professor in the Department of Computer Science and Engineering. John and his research group developed the Field programmable Port Extender (FPX) to enable rapid prototype of extensible network modules in Field Programmable Gate Array (FPGA) technology. Over the past 20 years, John has published over 100 papers and has 7 patents related to FPGA systems and networking systems. John earned his MS, BS, and PhD degrees from the Department of Electrical and Computer Engineering at the University of Illinois.

Arch Robison, Senior Principal Engineer, Intel. Arch Robison was the original architect of Intel Threading Building Blocks. He currently works on Intel Cilk Plus and is one of the authors of the book Structured Parallel Programming. He was the lead developer for KAI C++, and previously worked at Shell on massively parallel codes for seismic imaging. Arch holds a Ph.D. in computer science from the University of Illinois, 15 software patents, 3 winning entries in the International Obfuscated C Code Contest, and an Erdös number of 3.

Sanjay Shah, Founder & CTO, NanoSpeed. Sanjay has a career spanning 25 years in the UK and Europe. His experience includes: Lead Engineer for Fixnetix, a financial services company in London; Led a team of 10 senior engineers to develop FPGA Trading Gateway product for the UK and US markets; FPGA team lead for Airbus A350 engine control, safety and management (UK and France); Principal Architect of SharpEye Radar at Kelvin Hughes (UK); Founder and CTO of Sancom Technologies (Ireland) involved in Wi-Fi chip design; Senior member of team at Texas Instruments (France) developing 3G Telecoms products; and Senior member of DVD chip development team at Philips (Belgium). Sanjay holds degrees in Electronics from Imperial College, London and Cardiff University, UK.

Shawn Sloves, Founder and Partner, Atlas ATS, Inc.. Shawn is a founder and a partner of Atlas ATS Inc. a Global Digitial Currency Exchange and the Chief Executive Officer and Co-founder of Fundamental Interactions. Prior to joining the firm, Shawn was Co-founder and Head of Product & Strategy at Mantara Inc. In his five years at the firm he developed a suite of low latency trading infrastructure products widely deployed across high frequency trading firms and backed by over $40 million in invested venture capital. Prior to Mantara, as SVP at SunGard, Shawn ran product management and development for their market making direct access platforms that were widely deployed across teir one brokers. In addition, he was the product manager of the BRUT ECN, and he worked at Optimark Technologies. He has over 20 years of experience in the financial services industry. Shawn holds undergraduate degrees from Ohio State University and University of Massachusetts at Lowell, and a graduate degree from Montclair State.

Glenn Wright, Systems Architect, DataDirect Networks. Glenn has 20+ years of technical experience in the High Performance Computing industry, working on both server, networking and storage elements of extreme performance solutions. Glenn has been with DataDirect NetworksTM (DDN) for the last 3 years, during which time he has helped clients across HPC industries solve the new "big data" high performance/low latency problems. Glenn has recently focused on technical infrastructure solutions in high capacity analytics for environments with the need for extreme levels of I/O between the storage and server components of the solution. Prior to DDN, Glenn was a senior architect at QLogic (Infiniband group) and also held many varied/international roles at Sun Microsystems. 10/2013