STAC™ BENCHMARK COUNCIL

STAC® Summit

December 4, 2013
Doors open: 9:30am
Meeting starts: 10:00am

Hyatt Andaz Hotel
Great Eastern Room
40 Liverpool Street
London

Platinum Sponsors:

Gold Sponsors:

Lunch Sponsor:

Break Sponsor:

AGENDA

Note: Times are approximate.

BIG WORKLOADS

STAC Update – Big Workloads [slides]

- *Peter Lankford, Founder & Director, STAC*

STAC will review progress on Council activities related to workloads involving big data and big compute.

Parallel File Systems

- *Indulis Bernsteins, Storage System Architect - GPFS Expert, IBM* **[slides]**
- *Dan Ferber, Sr Manager, Systems Engineering, Intel* **[slides]**
- *Glenn Wright, Systems Architect, DataDirect Networks* **[slides]**

Parallel file systems are starting to get significant attention on Wall Street, and it's no surprise. Whether searching for alpha or quantifying risk, each trading firm has more and more compute nodes trying to access large data stores simultaneously. Data bottlenecks are rife. Parallel file systems--many of which hail from supercomputing--seem to promise great acceleration for data-intensive analytics. A panel of experts will offer their views.

Innovation Roundup – Round 1

"Next generation technologies for virtualized workloads: An Overview of the Solarflare SFN7122F 10/40GbE Server Adapter" [slides]	*David Riddoch, Chief Architect, Solarflare Communications*
"RDMA for the Masses" [slides]	*Richard Hastie, Director UK Financial Services, Mellanox Technologies*
"Vertically Scaling Messaging Systems to Meet the Needs of Big Data" [slides]	*Dave Clare, Regional Vice President, Solace Systems*

New approaches to real-time risk and reporting

- *Daniel Roberts, Solutions Architect, MongoDB* **[slides]**

Today's risk and compliance managers live in a new world. This world relies heavily on pre-deal, on-demand risk management, as well as regulatory reporting that can respond to changing regulator demands. But let's face it: not all firms are equipped for this world. Many are constrained by rigid architectures that make adaptation slow and expensive. In this talk, Daniel will discuss some of the key requirements for proactive risk controls, aggregated risk on demand, and adaptive regulatory reporting. He will then present a point of view on the best way to meet those requirements in a cost-effective way.

Networking Luncheon

Streaming data collection and the Internet of Things

- *Louis Polycarpou, Messaging Product Specialist Team Lead, Informatica* **[slides]**

As financial firms pursue big data analytics, many of them find that some of the information they need to integrate streams in from a variety of sources. And financial firms aren't alone. Companies in many industries see similar value in the event-driven side of big data. Some of the fastest growing use cases are associated with the so-called Internet of Things--the rapidly proliferating set of intelligent, Internet-connected consumer and commercial devices, each of which emits streams of machine-generated data that can be valuable when analyzed in conjunction with other data silos. But integrating streaming data into a big data architecture is often easier said than done. In this talk, Louis will discuss relevant use cases in capital markets and other industries, explain the challenges and limitations of existing technical approaches, and present Informatica's point of view on the best way to solve this important problem.

STAC-A2 on NVIDIA **[slides]**

- *Peter Lankford, Founder & Director, STAC*

STAC will unveil the results of audited STAC-A2 Benchmarks of a system using NVIDIA GPUs.

The Future of Accelerated Computing

- *John Ashley, Senior Solutions Architect, NVIDIA* **[slides]**

In NVIDIA's point of view, big data and big compute workloads increasingly expose the limitations of one-size-fits-all system designs. According to this view, energy is rapidly becoming the key driver in performance and operations, meaning that the ability to architect, deploy, and operate systems with a mix of general and more special purpose hardware will allow flexible enterprises to reap significant benefits to the top line from enhanced capability and to the bottom line from enhanced efficiency. In this talk, John will explore a near future in which systems commonly embrace heterogeneity and appropriate specialization, from processors through to storage and networking. In particular, he will focus on the energy cost of moving data around the datacenter and within the server, and lay out the benefits of hardware and software that move compute closer and closer to data.

FAST WORKLOADS

STAC Update – Fast Workloads **[slides]**

- *Peter Lankford, Founder & Director, STAC*

STAC will review progress on Council activities related to low-latency, high-volume realtime workloads

Technical Brief: Getting the most from Haswell

- *Jim Cownie, Principal Engineer, Intel* **[slides]**

The first of Intel's Haswell processors has been released to the market, with more on the way. This architecture supports new intrinsics and the Haswell New Instructions, which have the potential to reduce latency and accelerate compute- and data-intensive workloads. Jim will provide insight into the most promising of these innovations and where developers should focus their initial efforts.

Innovation Roundup – Round 2

"Achieving Ultra-Low Latency Tick-to-Trade Performance With Mainstream Technology" **[slides]**	*Mark Skalabrin, CEO, Redline Trading Solutions*
"Embracing Open Source in the Enterprise" **[slides]**	*Scott Lasica, VP, Global Alliances, Rogue Wave Software*
"TIBCO FTL: Still the Fastest and now the Broadest" **[slides]**	*John Page, Global Director Messaging, TIBCO*

Coffee Break

New frontiers in latency, determinism, and transparency

- *Dr. Martin Zinser, Head of Trading Interfaces, Eurex Frankfurt AG* **[slides]**

Eurex recently launched its T7 system, which dramatically reduced latency, improved predictability, and enhanced performance transparency for market participants. Martin will discuss this new architecture, the thought process that led Eurex to it, and where it is headed.

Innovation Roundup – Round 3

"New Enhancements in Precision Time, Instrumentation, and Packet Capture with the Solarflare SFN7322F IEEE 1588 Precision Time Server Adapter" **[slides]**	*Martin Porter, VP, Software Development, Solarflare Communications*
"Building highest density networks at lowest latency" **[slides]**	*Shyam Srinivasan, Product Manager, Cisco*
"Shaving nanoseconds: pushing the frontiers of low latency networking" **[slides]**	*Matthew Grosvenor, Staff Engineer, Exablaze*
"Making the Invisible Visible in ULL Networks" **[slides]**	*Sean Flack, Senior Systems Engineer, EMEA, Arista Networks*
"MetaConnect - The 4 nanosecond layer 1 switch with dynamic patching, media conversion, tapping, monitoring and timestamping." **[slides]**	*David Snowdon, Founder, co-CTO, Metamako*

Hardware acceleration today

- *Antonio Roldao, EAI Accelerator Group, Morgan Stanley*
- *Nikolaj Hermann, CTO, Fiberblaze* **[slides]**
- *Sanjay Shah, CTO, Nanospeed Technologies* **[slides]**

Seven years after the first well-known use of FPGA to accelerate financial workloads, what is the state of the art? Where does FPGA play in the trading process? What is the division of labor between vendors and internal staff? Where can we expect the technology to head? And hey: with all the talk of the latency race being "over", why are we still talking about FPGA?

Networking Reception

Speaker Biographies – Feature Sessions

John Ashley, Senior Solutions Architect, NVIDIA. John is NVIDIA's Senior Solutions Architect covering global financial services customers. His background is best described as "varied", with degrees in Electrical Engineering, a US Patent in predictive analytics, and an IT career as a developer, DBA, systems architect, and project manager working for a variety of end user, vendor and consulting firms in the government and financial sectors. He is currently based in London.

Indulis Bernsteins, Storage System Architect, IBM. Indulis has been a technical specialist and systems architect at IBM for over 30 years. His experience covers designs and projects implementing solutions built from a range of technologies- storage, servers, clusters, and networks- across a diverse set of industries and customers- including banking, retail, government, healthcare, and technical computing. For the last 4 years he has specialised in High Performance Computing systems (with one system currently #48 in the top500 computer list), and is currently the European technical lead architect for IBM's GPFS parallel filesystem, covering both commercial and technical uses.

Jim Cownie, Principal Engineer, Intel. Jim is an Intel principal engineer and is currently architect for the OpenMP runtime. He has worked on parallel computing since 1979 when he started at Inmos working on Occam and the Transputer. He served on the HPF and MPI committees, designing the MPI profiling interface as chair of the MPI-1 profiling sub-committee. Since joining Intel eight years ago, amongst other things, he has worked on the Pin profiling infrastructure, Intel® Transactional Synchronization Extensions (Intel® TSX) and OpenMP. He lives in Bristol, and would rather be skiing.

Dan Ferber, Sr Manager, Systems Engineering, Intel. Dan leads the Systems and Solutions Engineering team for Lustre at Intel. He is responsible for supporting Intel's Lustre community partners and customers in HPC and moving Lustre into Exascale. Dan previously ran Business Development and Strategic Partnerships at Whamcloud, a Lustre start-up acquired by Intel in July, 2012. Prior to Intel and Whamcloud, Dan had more than 20 years of high tech experience developing and supporting HPC communications software, configuration management tools, database software, I/O libraries and commercial software at Cray, SGI, Sun, and Oracle. He also managed engineering, support, and business development teams. Dan holds a Master's degree in Computer Systems from the University of St. Thomas in St. Paul, Minnesota, a Bachelor's degree from Occidental College in Los Angeles, and attended Phillips Exeter Academy in Exeter, New Hampshire. He has lived a year each in London, England and Barcelona, Spain and is permanently based in Minnesota. Dan's focus in on meeting customers' needs.

Nikolaj Hermann, CTO, Fiberblaze. Nikolaj has been in charge of the development of the complete product portfolio at Fiberblaze, including all 10 GigE FPGA based Network Interface Cards. The network interface cards are now being used as the state-of-the-art choice at many High Frequency Trading sites worldwide. Before Nikolaj founded Fiberblaze in 2008, he worked in the electronics and telecommunication industry for more than 10 years and holds a degree in physics.

Peter Lankford, Founder & Director, Securities Technology Analysis Center. Peter has overseen STAC since its birth in 2006. Before that, Peter was SVP of Information Management Solutions at Reuters, where he led the $240M market data systems business. Peter's team led Reuters into the business of low-latency direct feeds and catalyzed the widespread adoption of Linux on Wall Street by making RMDS available on that platform. Prior to Reuters, Peter held management positions at Citibank, First Chicago Corp., and operating-system maker IGC. Peter has an MBA, Masters in International Relations, and Bachelors in Chemistry from the University of Chicago.

Daniel Roberts, Senior Solutions Architect, 10gen. Daniel leads the Solutions Architecture team for Financial Services at 10gen (the MongoDB company) supporting Europe, Middle East and Africa. Prior to 10gen, Daniel worked at Oracle for 11 years in a number of different positions focusing mainly around Oracle's middleware technologies and strategy. His prior roles have included consulting, product management, business development and pre-sales. Daniel has also worked for Novell, ICL and for a period as a freelance contractor. He has a degree in Computer Science from Nottingham Trent University in the UK.

Louis Polycarpou, Messaging Product Specialist Team Lead, Informatica. Louis is the Ultra Messaging Product Specialists Team Lead at Informatica, and has 15 years experience working in flexible roles involved in all stages of bespoke development, product delivery and sales. He primarily has a financial-services led consulting background but also has extensive experience in product development, conducting and assisting the pre-sales function and is a specialist in the areas of Java development and the messaging and systems integration space.

Dr. Antonio Roldao, EAI Accelerator Group, Morgan Stanley. Antonio holds a Ph.D. in High-Performance Computing using Field Programmable Gate Arrays, from Imperial College London. Having started using FPGAs 10 years ago in the aerospace industry, Antonio is now applying this technology in finance. Within Morgan Stanley he is responsible for MS's proprietary Rapid-Hardware Development platform, core libraries, and provides internal consultancy services. Prior to Morgan Stanley, Antonio worked at J.P. Morgan where he bridged Maxeler's FPGA-based solution with the Athena Platform. Beyond FPGAs, Antonio is also interested in a wider range of technologies and maintains the World's Largest Collaborative Painting - WebCanvas.com

Sanjay Shah, Founder & CTO, NanoSpeed. Sanjay has a career spanning 25 years in the UK and Europe. His experience includes: Lead Engineer for Fixnetix, a financial services company in London; Led a team of 10 senior engineers to develop FPGA Trading Gateway product for the UK and US markets; FPGA team lead for Airbus A350 engine control, safety and management (UK and France); Principal Architect of SharpEye Radar at Kelvin Hughes (UK); Founder and CTO of Sancom Technologies (Ireland) involved in Wi-Fi chip design; Senior member of team at Texas Instruments (France) developing 3G Telecoms products; and Senior member of DVD chip development team at Philips (Belgium). Sanjay holds degrees in Electronics from Imperial College, London and Cardiff University, UK.

Glenn Wright, Systems Architect, DataDirect Networks. Glenn has 20+ years of technical experience in the High Performance Computing industry, working on both server, networking and storage elements of extreme performance solutions. Glenn has been with DataDirect NetworksTM (DDN) for the last 3 years, during which time he has helped clients across HPC industries solve the new "big data" high performance/low latency problems. Glenn has recently focused on technical infrastructure solutions in high capacity analytics for environments with the need for extreme levels of I/O between the storage and server components of the solution. Prior to DDN, Glenn was a senior architect at QLogic (Infiniband group) and also held many varied/international roles at Sun Microsystems.

Dr. Martin Zinser, Head of Trading Interfaces, Eurex Frankfurt AG. Dr. Martin Zinser, Head of Trading Interfaces, Eurex Frankfurt AG. Martin is responsible for the Units developing the transactional and GUI trading interfaces for the Eurex T7 trading system. He has been deeply involved in the technical setup, operations and monitoring aspects of the new system. He joined Deutsche Boerse more than 15 years ago, running for 10 years the technical operations team for Eurex and Xetra from Chicago. He is a nuclear physicist by education and in his free time tries to improve the latency of his run and bike times.